

MS-7680 Ver:3.3 m-ATX : 245 X 210mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61,Co-lay H67)

OnBoard Chipset:

HD Audio Codec:VT1708S Co-lay 1818S

LAN:AR8151B 10/100/1000 , Co-lay 8152B 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

PWM:

Controller:VRD12 UT501 4+1 Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT CPU SA

Controller:uP6103

DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x6

D-SUB *1

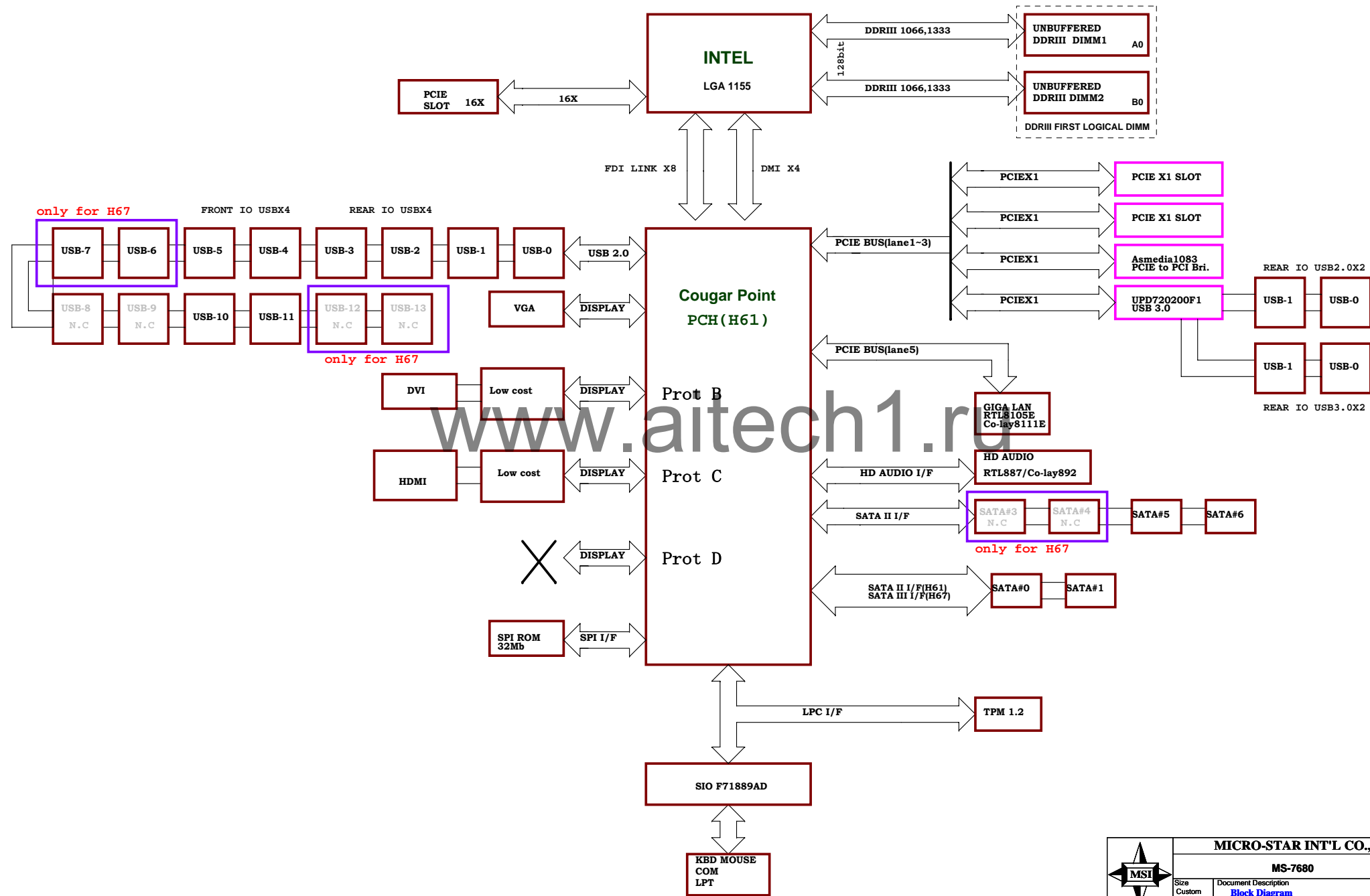
TPM Header *1

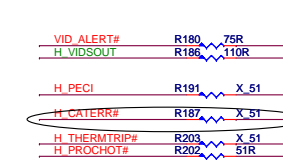
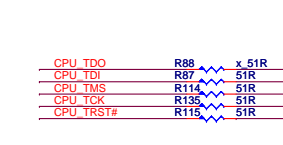
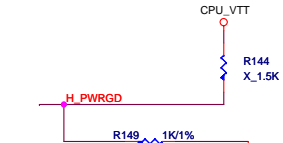
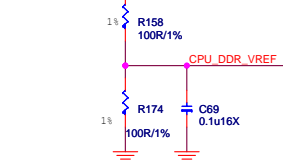
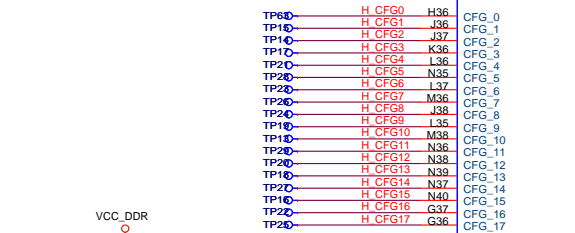
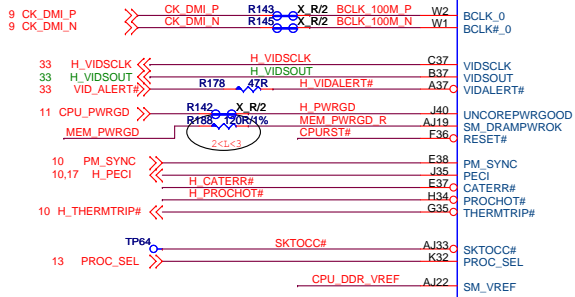
COM Header *1

LPT Header *1

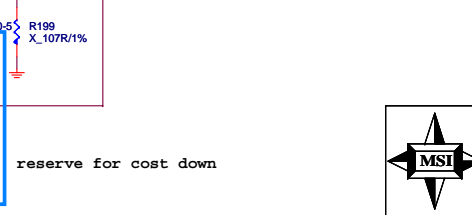
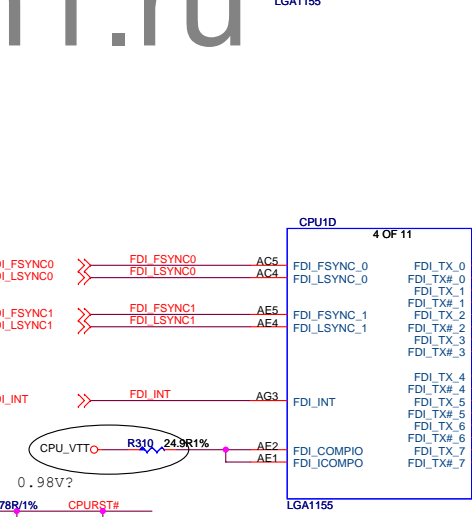
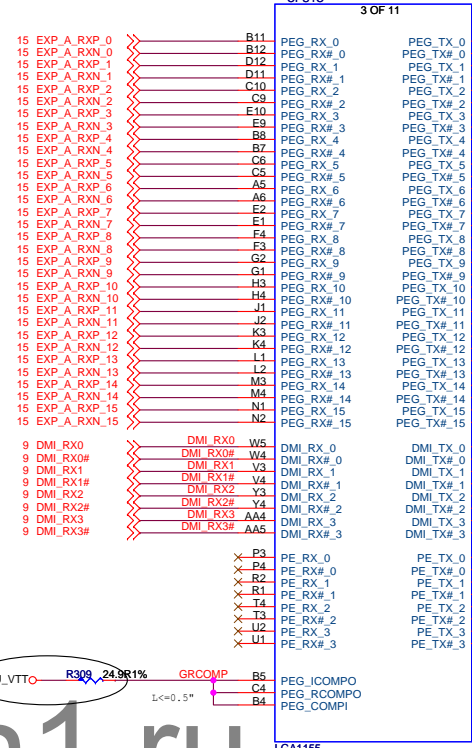
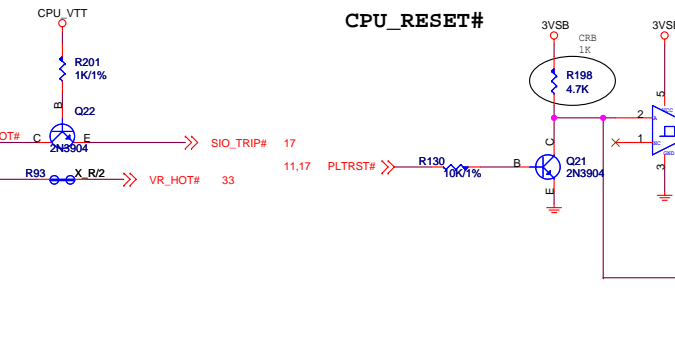
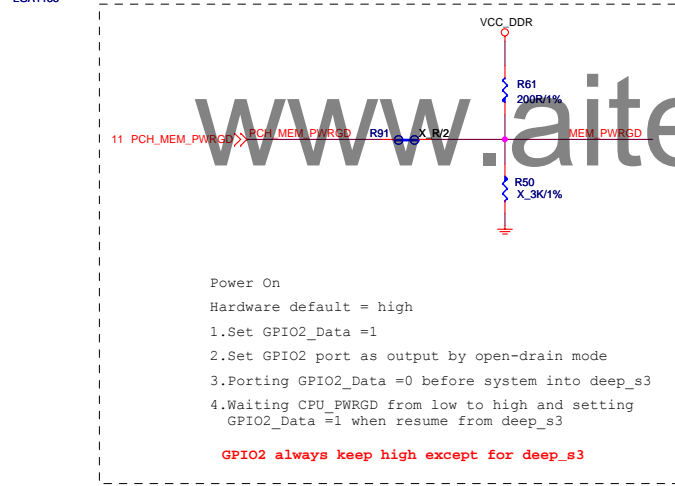
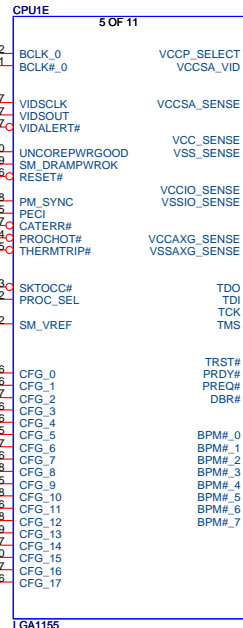
on BOARD BUZZER

Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG	3
CPU-Memory	4
CPU-Power	5
CPU-GND	6
DDR III DIMM 1	7
DDR III DIMM 2	8
CP-PCI/E/DMI/USB/CLK	9
CP-SATA/HOST/FAN/GPIO/VGA	10
CP-SMB/LPC/AUDIO/RTC	11
CP-POWER	12
CP-GND/NVRAM	13
CP Strap	14
PCIe x16 /x1 /x1HDA CO-LAY	15
PCIEx1 Slots	16
SIO-Fintek F71869AD(EUP)	17
LAN - AR8151B Co-lay AR8152B	18
VT1708S Co-lay 1818S	19
ASM1042 USB30	20
ASM1061 SATA 6G	21
VGA	22
SATA / FAN Control	23
USB Connector	24
ACPI Controller UPI	25
DDR Power - uP6103 1-Phase	26
PCH Power - uP6103 1-Phase	27
CPU_VTT - uP6103- 1-Phase	28
CPU_SA - OP+MOS	29
VRD12 - UT501 4+1-Phase	30
UP6282 2-Phase+MOS CPU	31
UP6282 1-PhaseMOS GPU	32
ATX F_Panel/EMI/TPM/LPT	33
XDP / Manual Parts	34

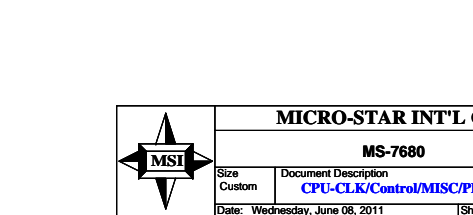
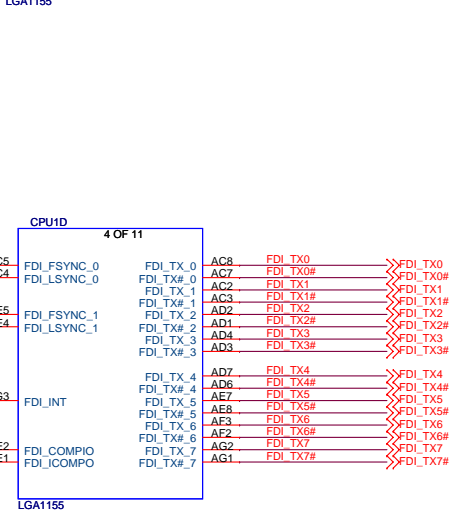
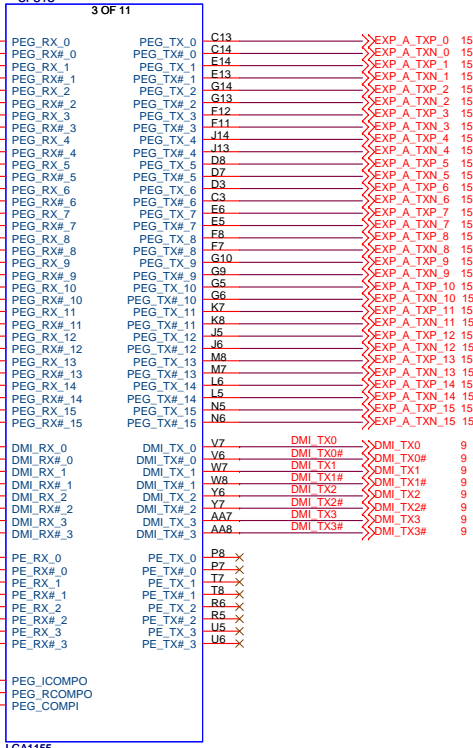




PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8



reserve for cost down



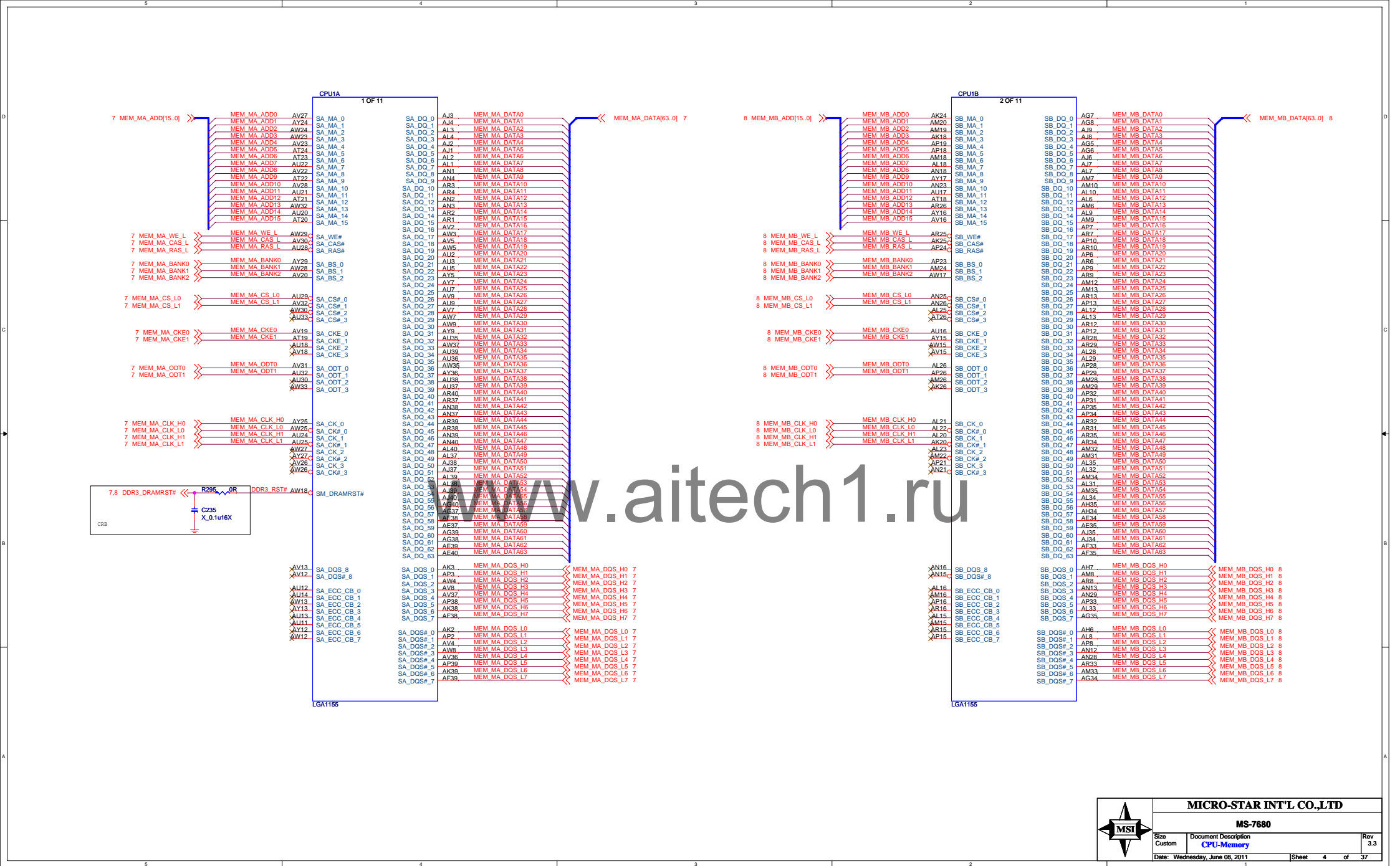
reserve for cost down

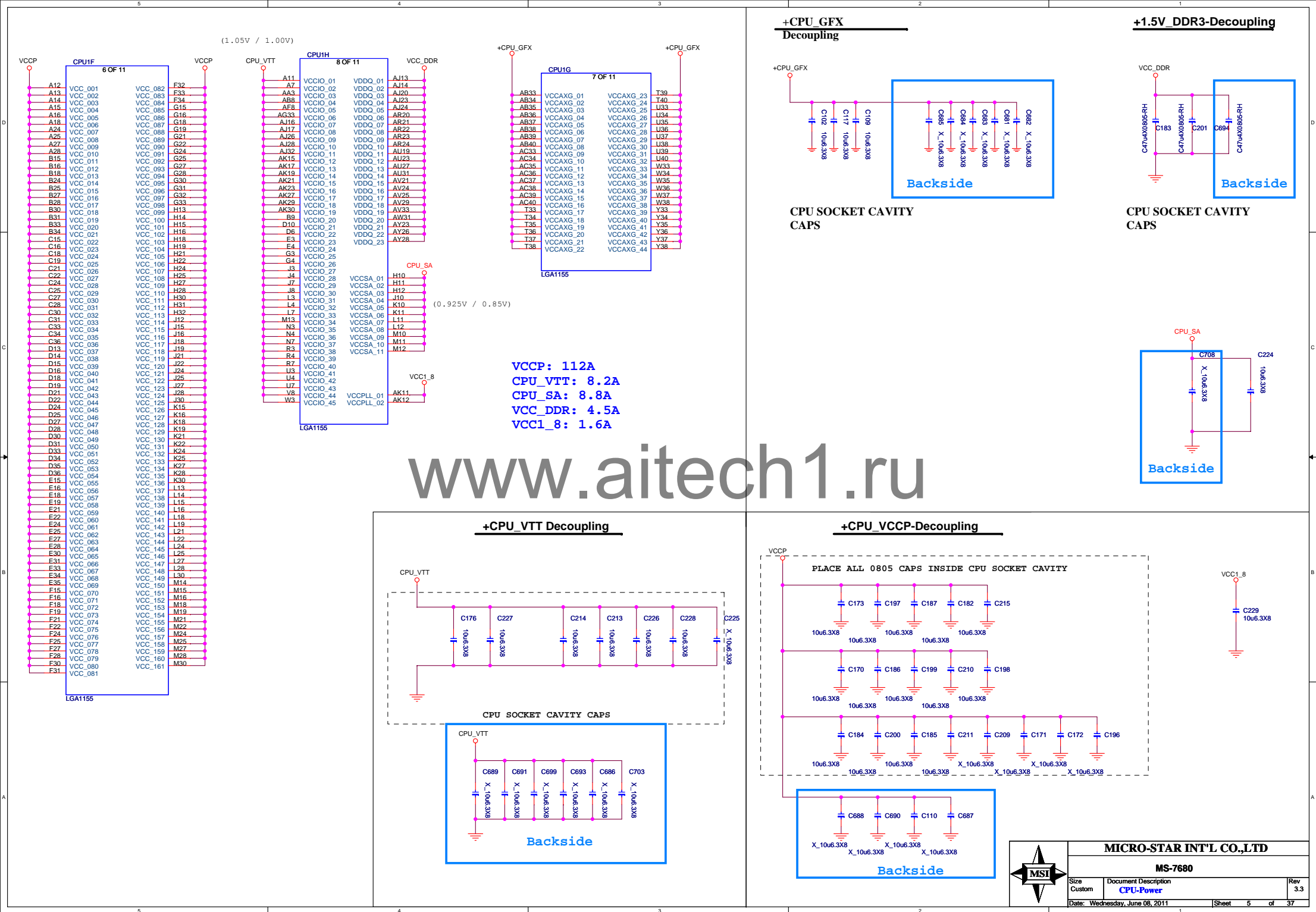
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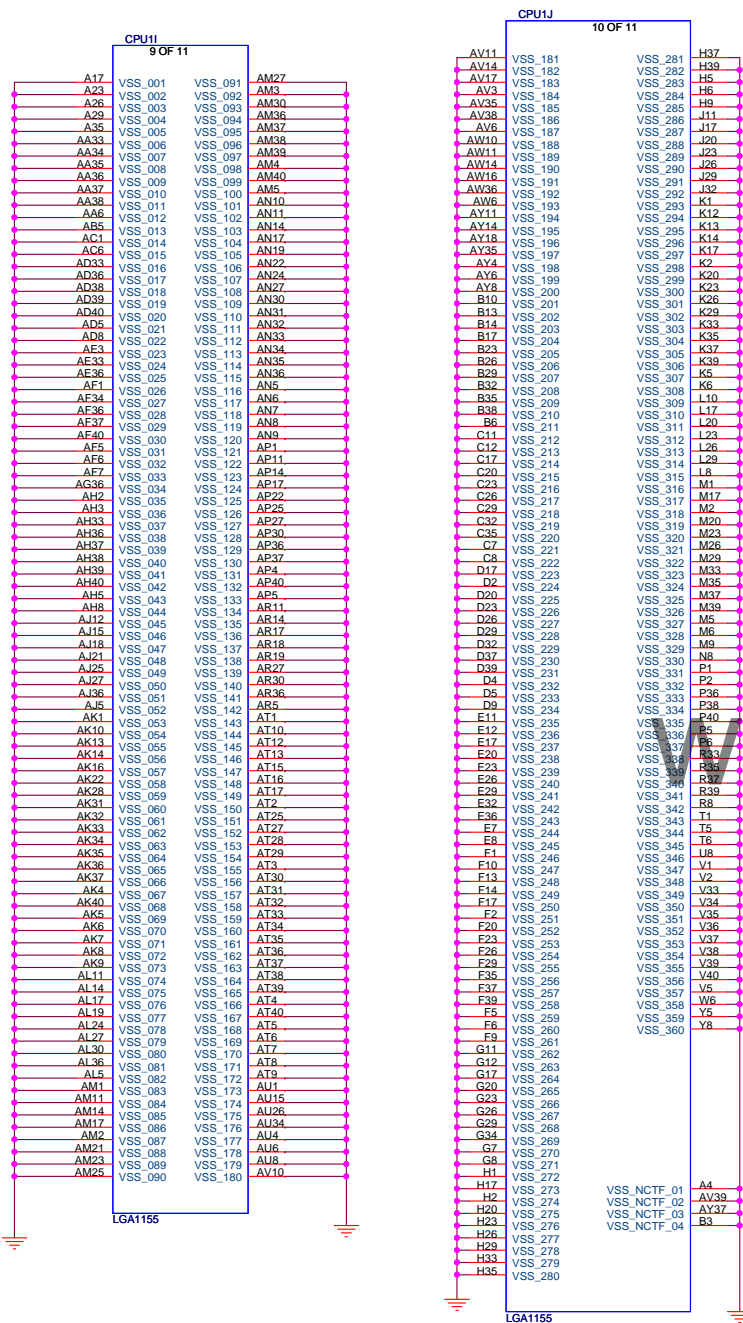
MS-7680

Size Custom Document Description **GPU-CLK/Control/MISC/PEG** Rev 3.3

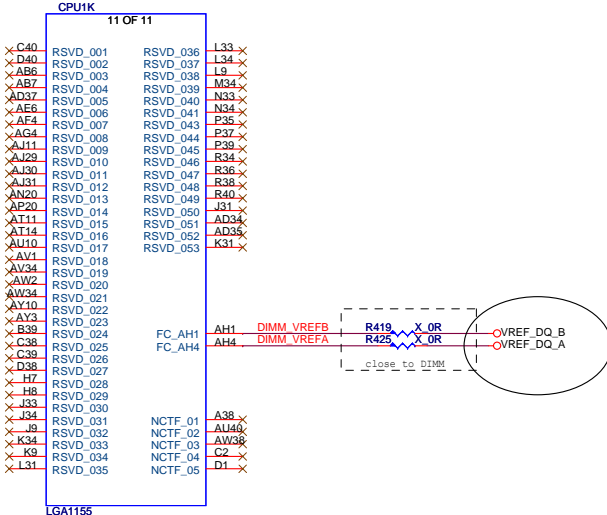
Date: Wednesday, June 08, 2011 Sheet 3 of 37







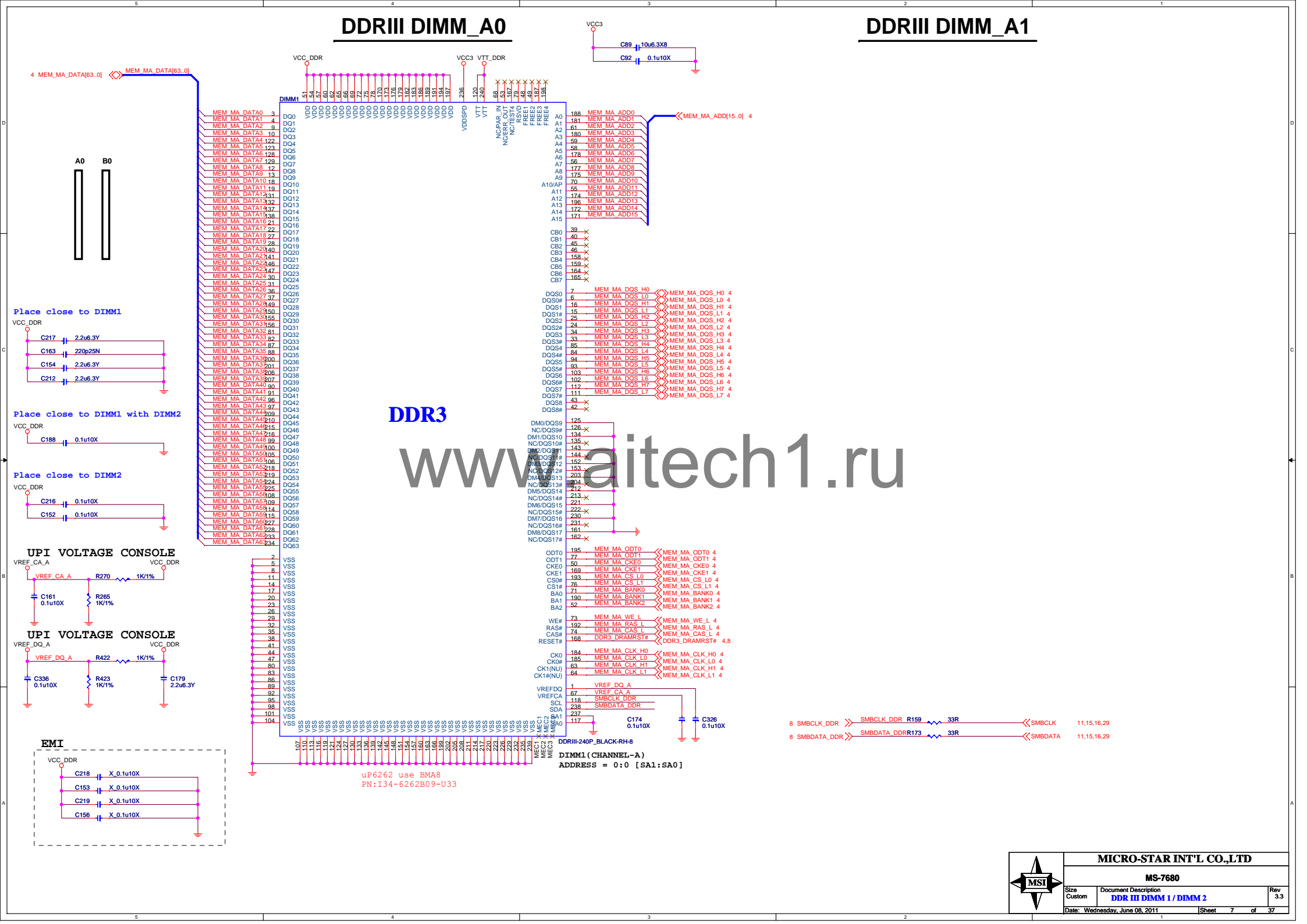
CRB 0.7 107 page



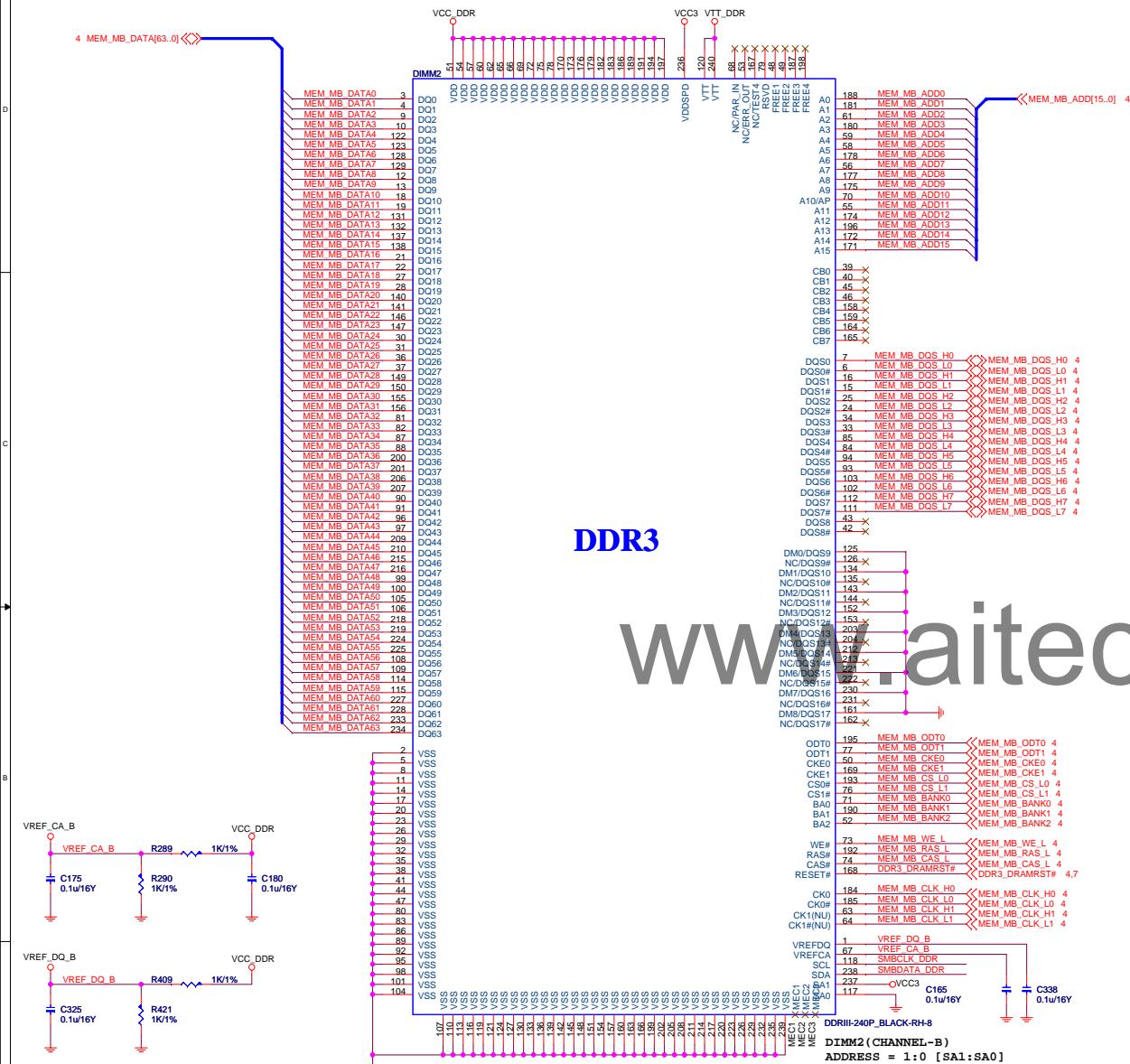
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DDRIII DIMM_A0

DDRIII DIMM_A1



DDRIII DIMM_B0



DDR3

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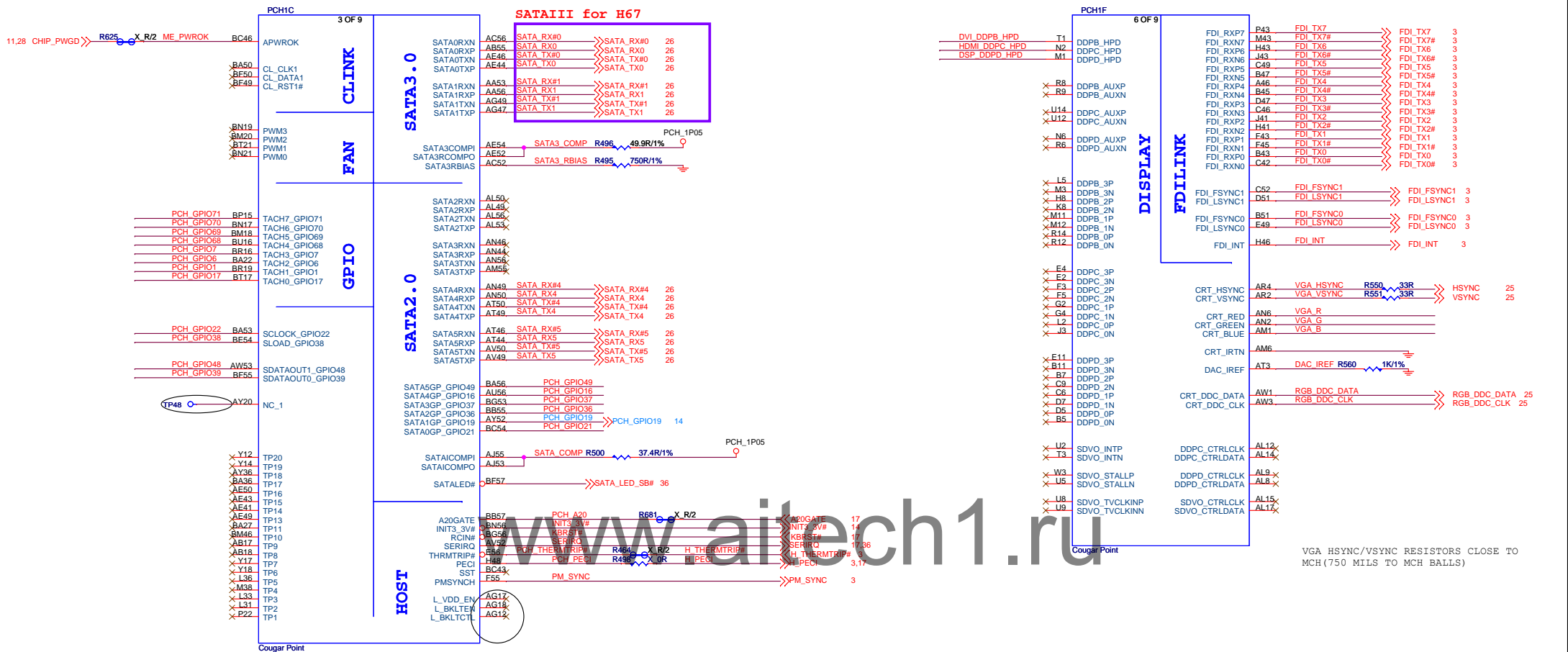
SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7



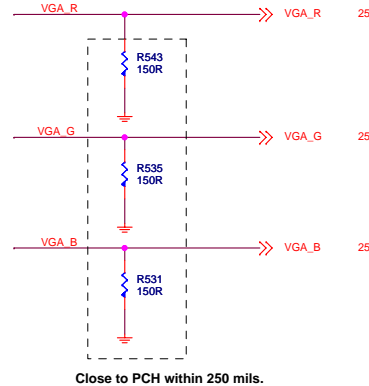
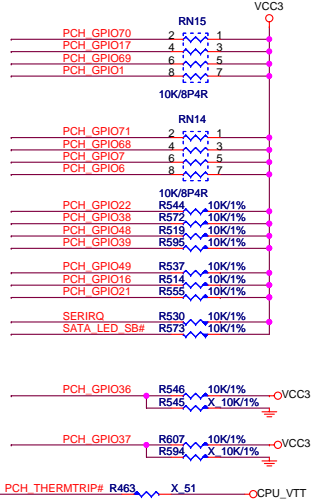
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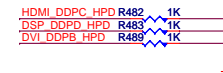
Size Custom	Document Description DDR III DIMM 3 / DIMM 4	Rev 3.3
Date: Wednesday, June 08, 2011		Sheet 8 of 37



Pull HIGH for PCH



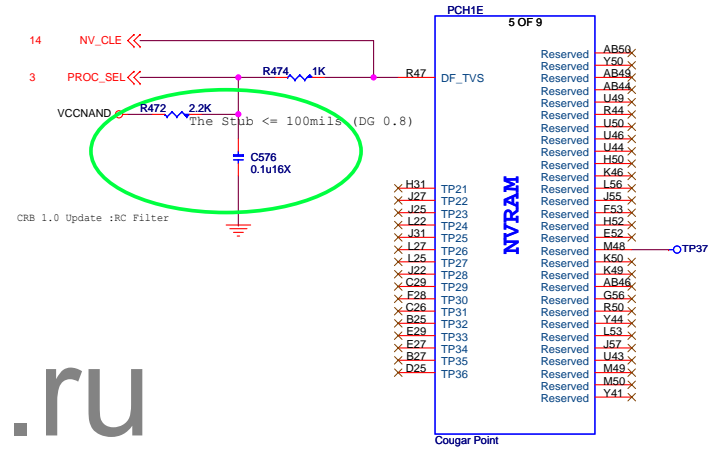
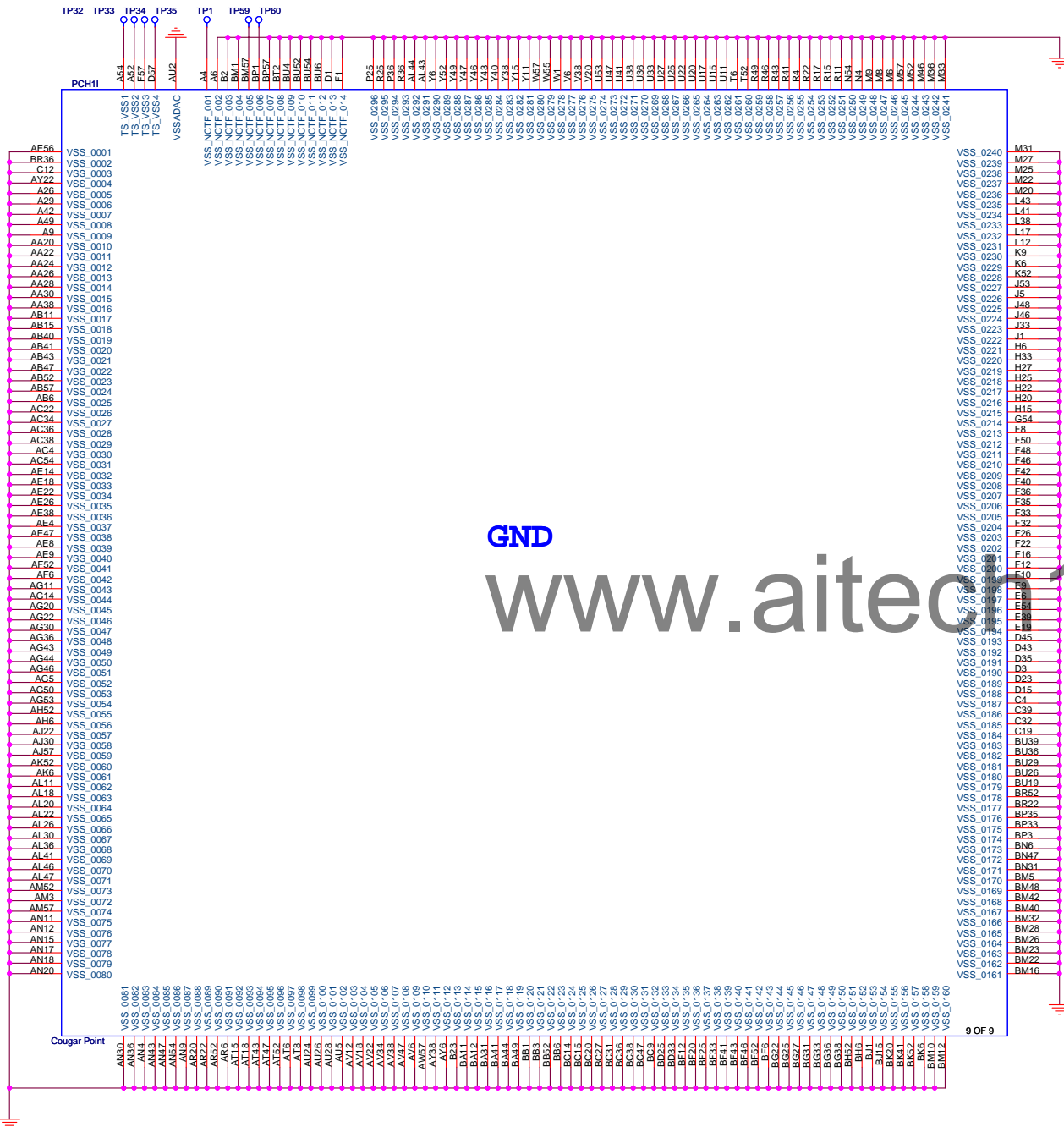
No VGA(pull down)



Enable VGA(CTRLCLK/DATA Pull High)

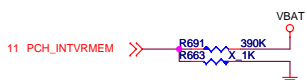
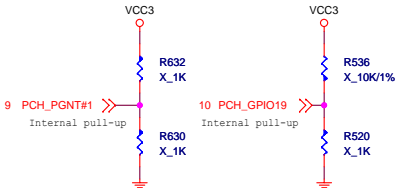


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MS-7680			
Size	Document Description		Rev
Custom	CP-SATA/HOST/FAN/GPIO/VGA		3.3
Date:	Wednesday, June 08, 2011	Sheet	10 of 37



PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



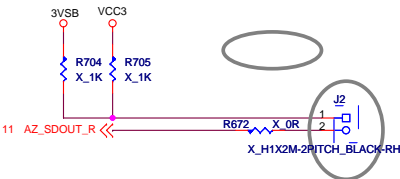
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



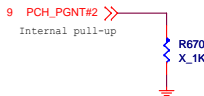
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

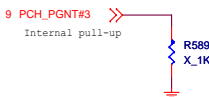


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

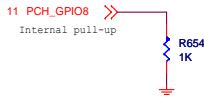
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



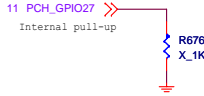
DMI AC/DC MODE
0 : AC
1 : DC *



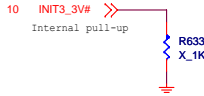
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up

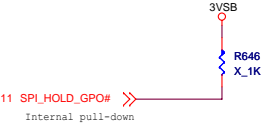


INT3_3V#
0 : ??????????????
1 : ?????????????? *

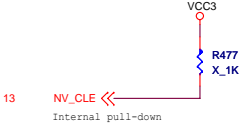
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



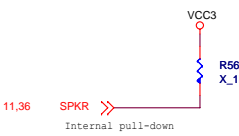
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY*
1: 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



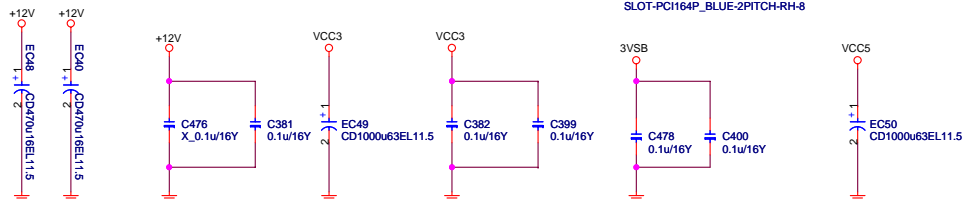
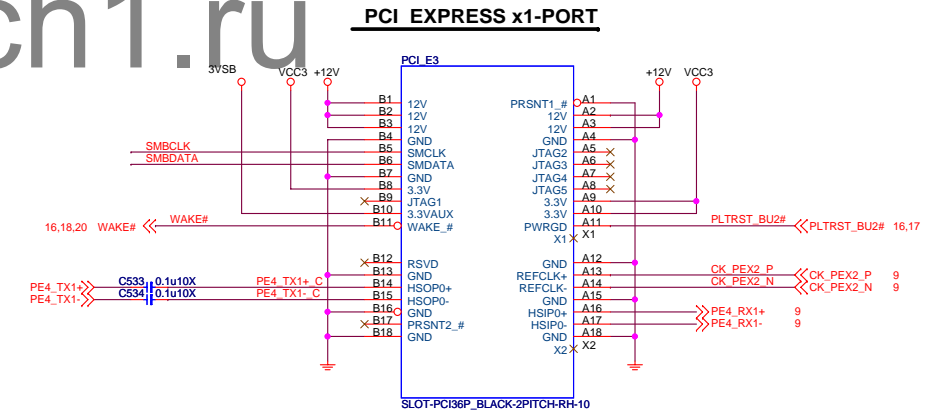
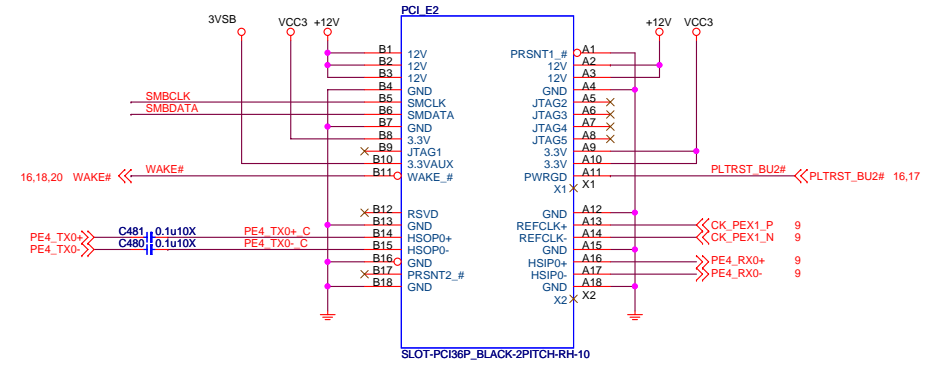
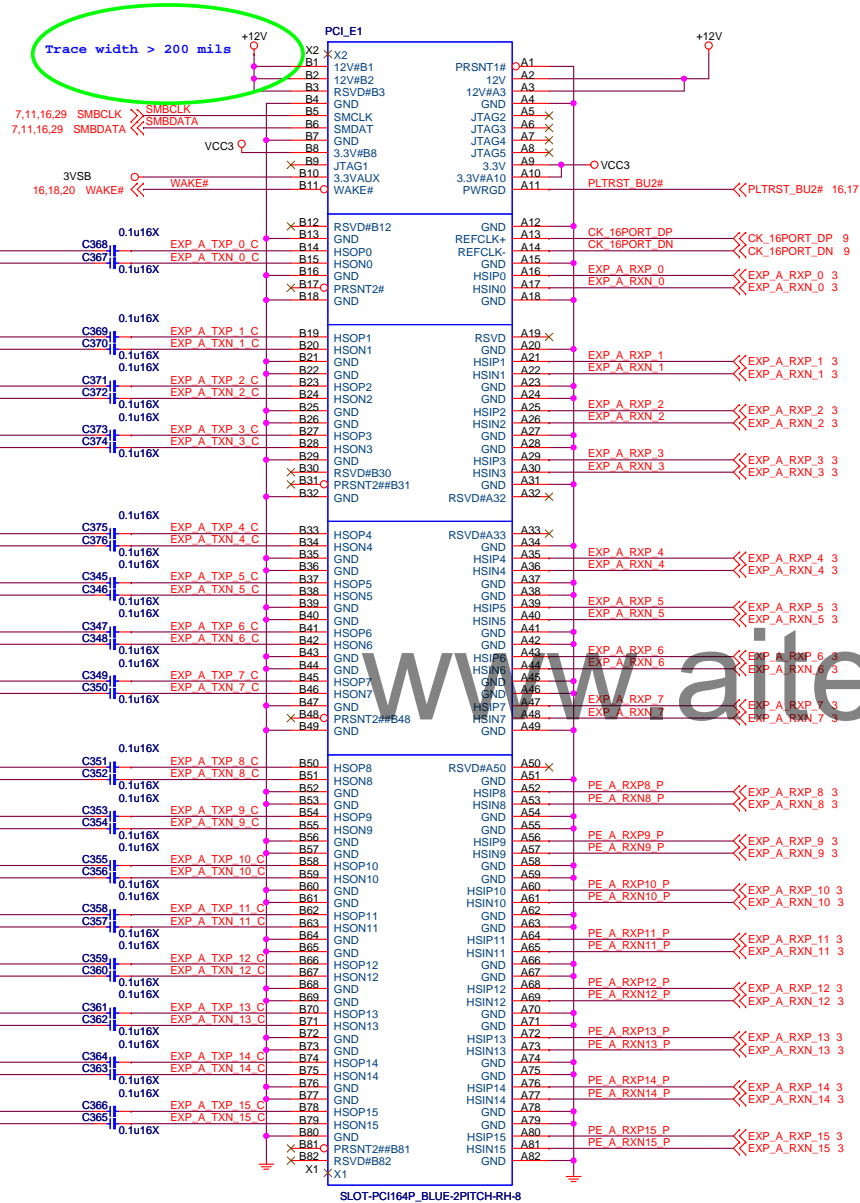
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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Size	Document Description	Rev
Custom	CP-Strap	3.3
Date: Wednesday, June 08, 2011	Sheet 14 of 37	

PCI_Express X16 Slot

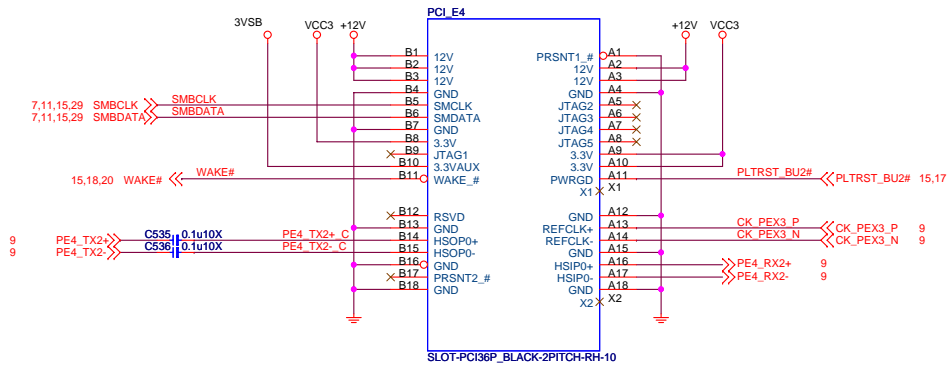


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MS-7680

Size Custom	Document Description PCIE x16 /x1/x1	Rev 3.3
Date: Wednesday, June 08, 2011	Sheet 15 of 37	

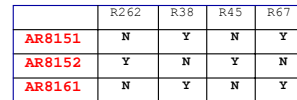
PCI EXPRESS x1-PORT



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	R471
AR8151	N
AR8152	N
AR8161	Y



	R81	R82
AR8151	Y	N
AR8152	N	Y
AR8161	Y	N

Place near pin1

Trace width >40mil

VDD3.3

3VSB

lencho

30

5,r36,r24

r26,c36,c37,c48,c47

9,R30,R28,R26,C48,C47

length <4"

edance=100 ohm

PLTRST_BU1#

R713

X_4.7K

VDDCT_REG

C118

C88

X_1u6.3Y4

D24

X_S-BAT54C_SOT23

R786

X_0/4

R790

0/4

SB_WAKE#

11

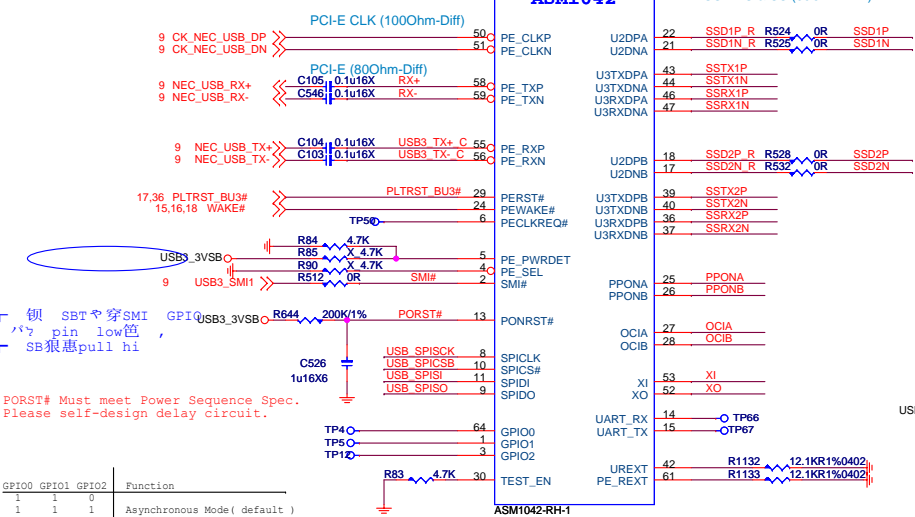
X_1u6.3Y4

Giga-Lan		10/100-Lan	
N58-22F0731		N58-22F0771	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19	Yellow	19	Yellow
20	Orange	20	Green
21	Green	21	None
22	None	22	Yellow

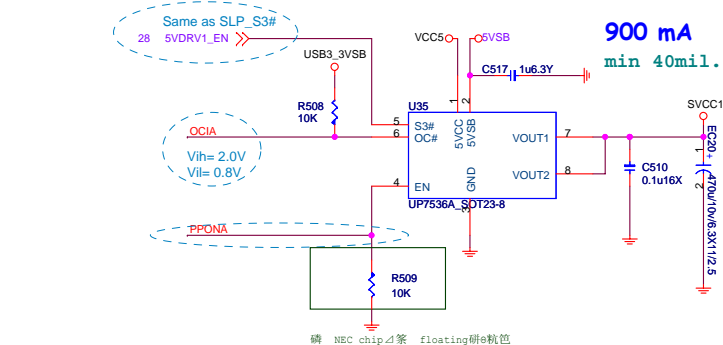
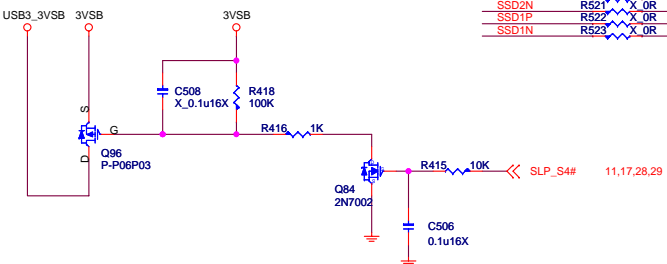


Size Custom	Document Description LAN - RTL8111E / 8105E	Rev 3.3
Date: Wednesday, June 08, 2011		Sheet 18 of 37

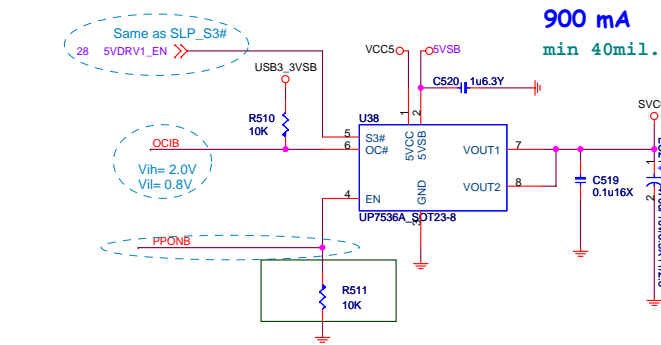
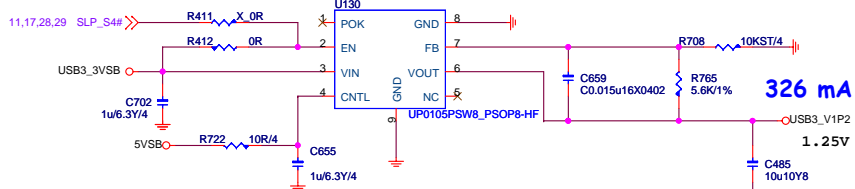
ASM1042 USB3.0



3V_Dual Circuit



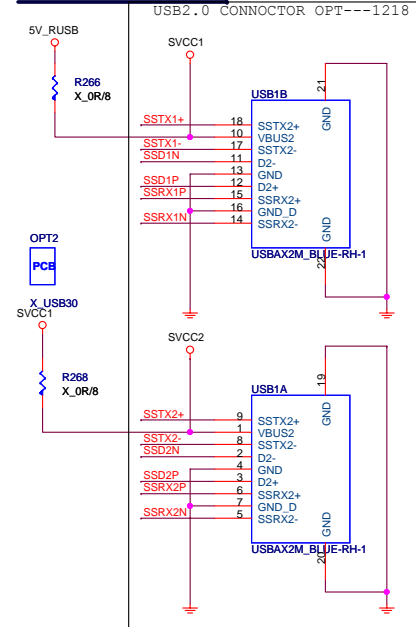
NEC chip floating pin



NEC chip floating pin

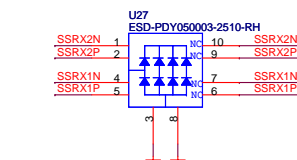
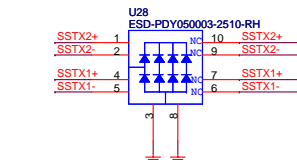
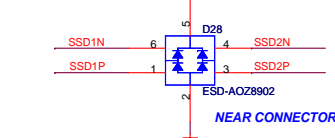
remove usb30 stuff

Rear USB3.0



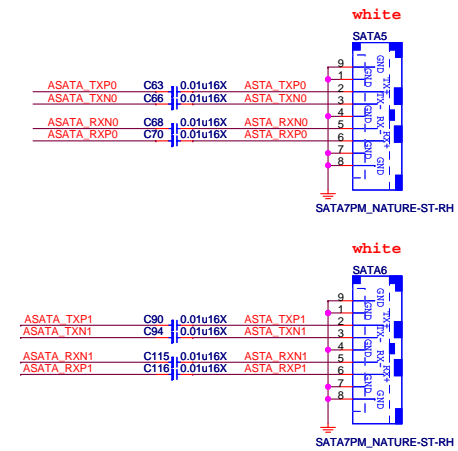
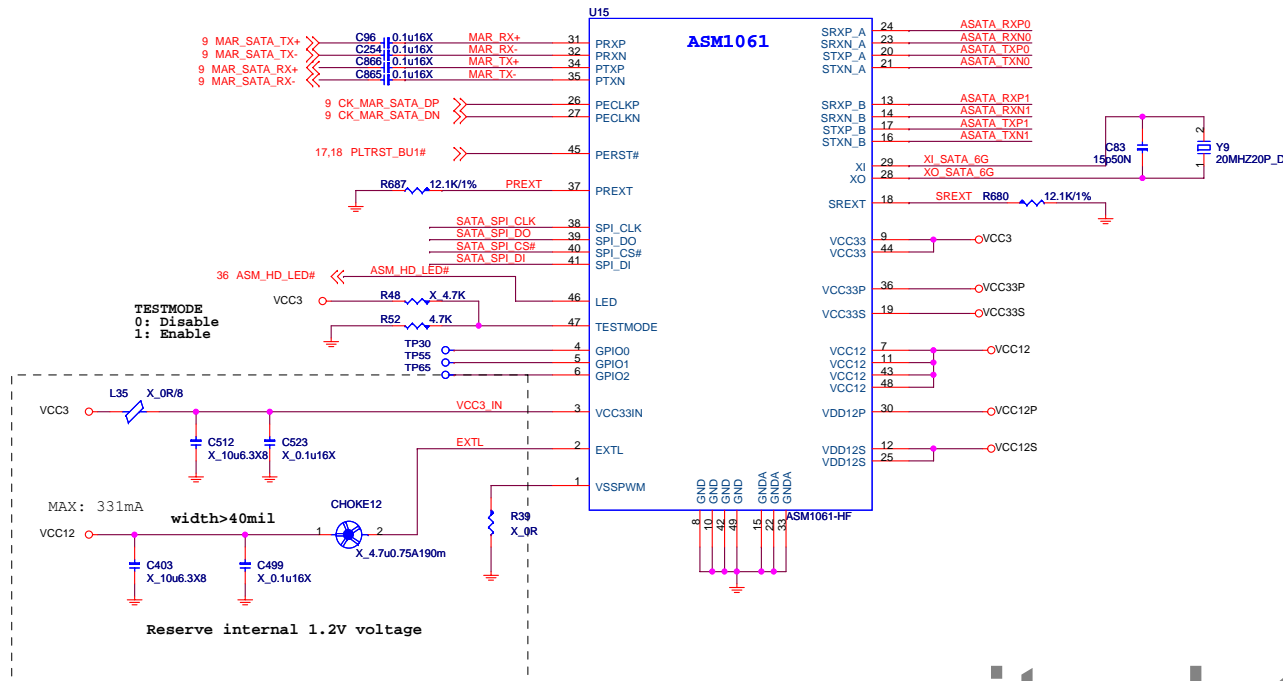
ESD Protection

Close to Connector



MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size	Document Description	Rev
Custom	ASM1042-USB 3.0	3.3
Date: Wednesday, June 08, 2011	Sheet 20 of 37	

ASM1061 SATA6G



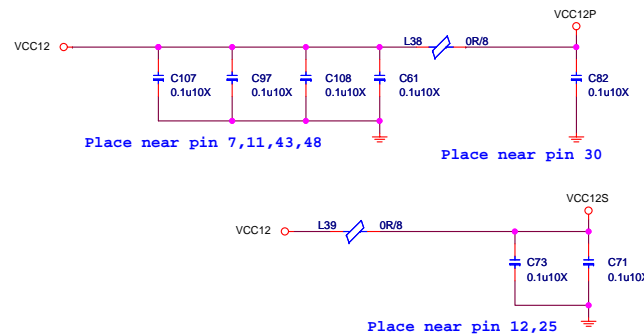
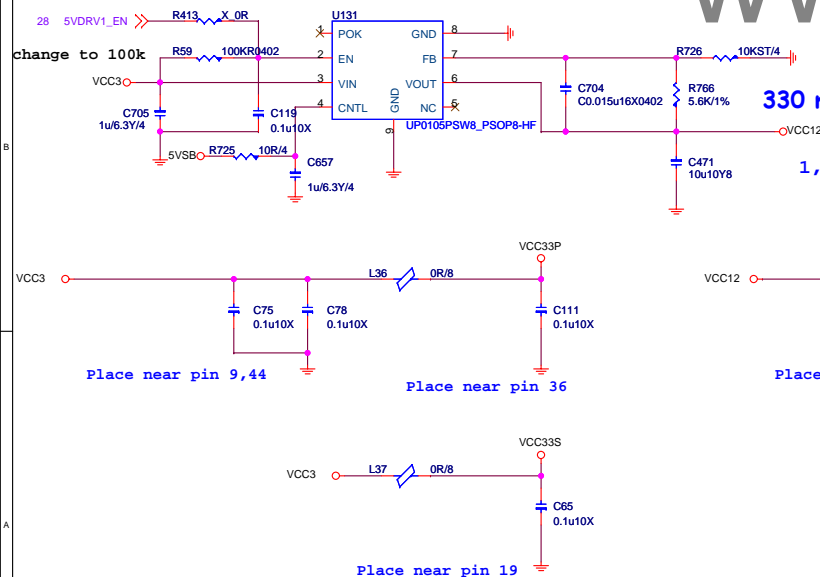
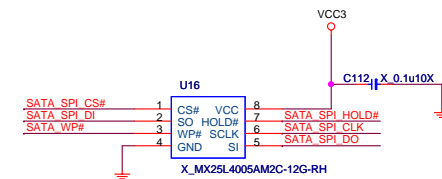
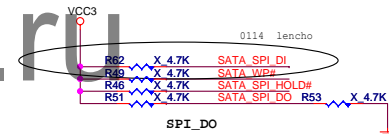
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ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

330 mA

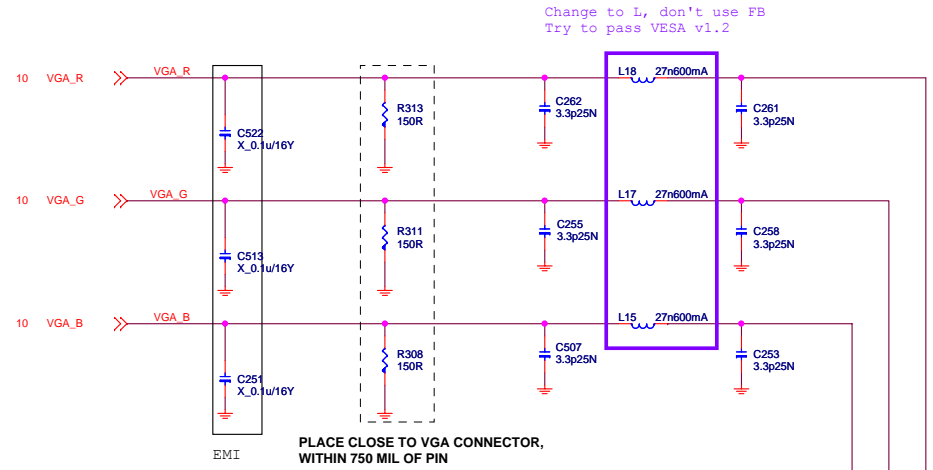
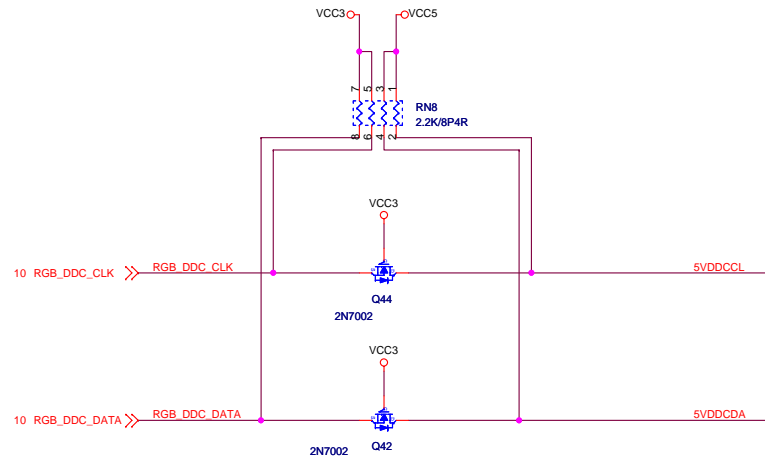
1,25V



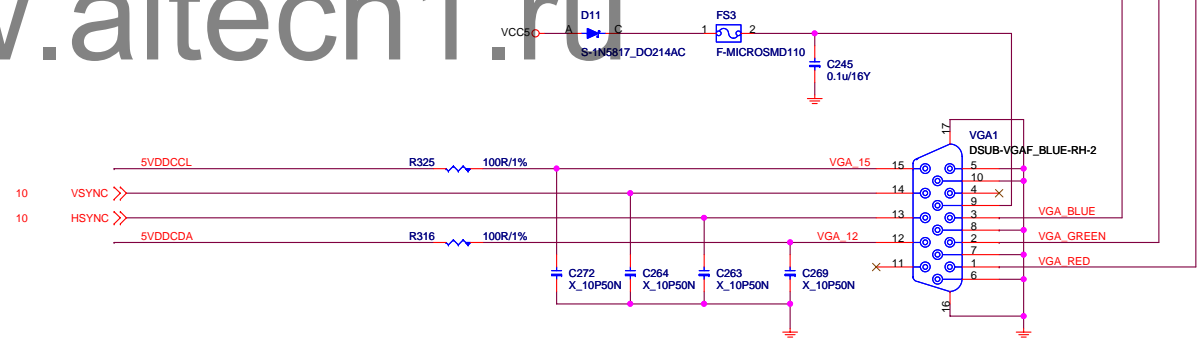
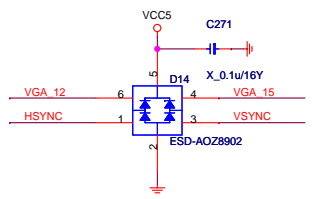
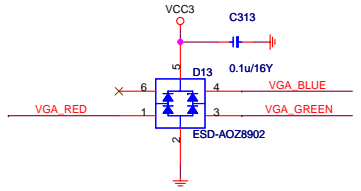
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

LevelShift

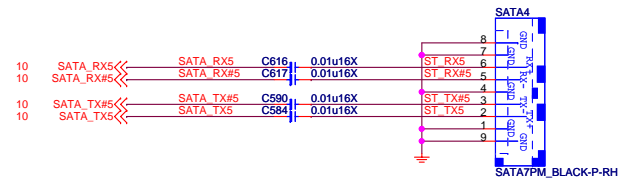
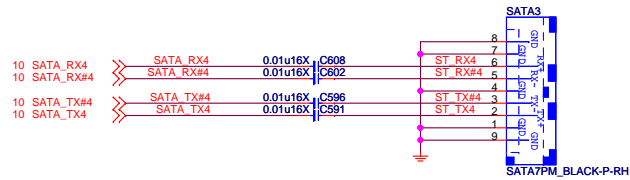
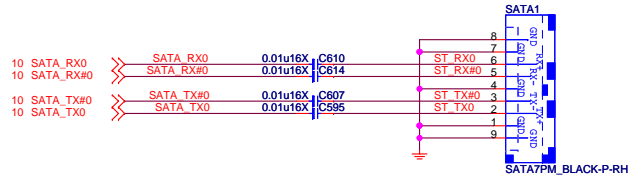


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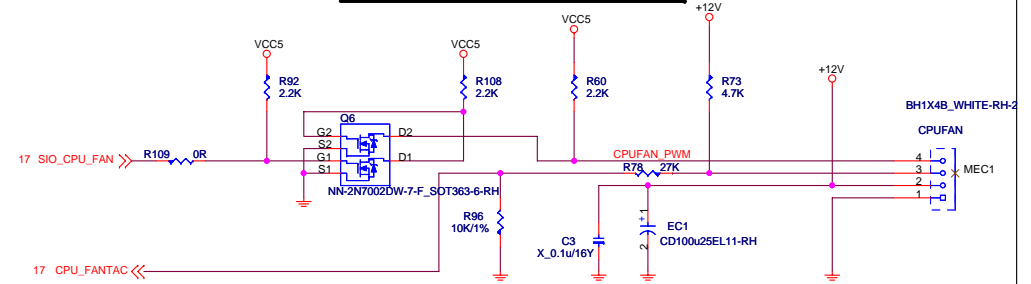


SATA 6G PORT 0,1

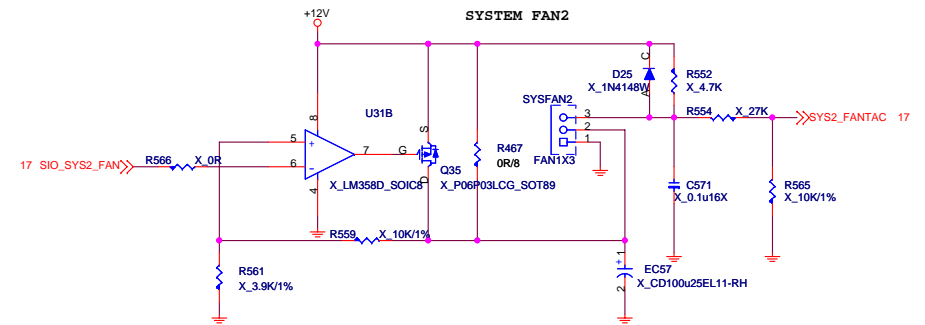
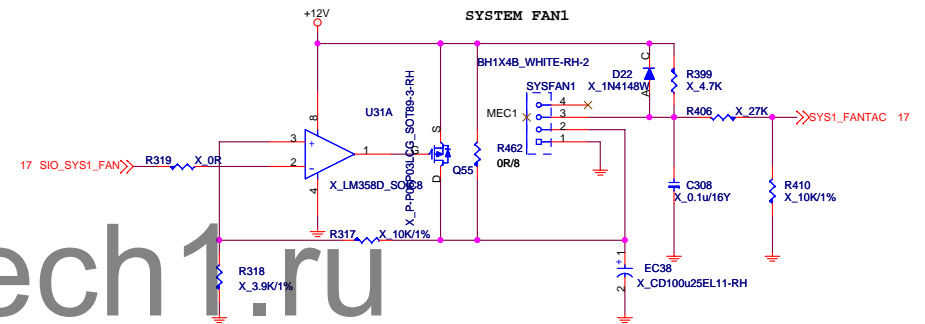
H61 PORT 0/1 3G
H67 PORT 0/1 6G



CPU FAN-COUNTROL CIRCUIT



SYSTEM FAN-COUNTROL CIRCUIT

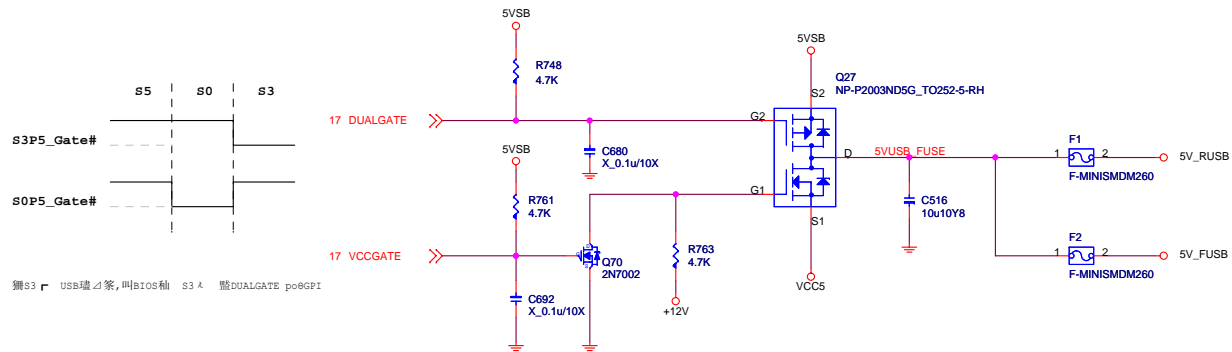


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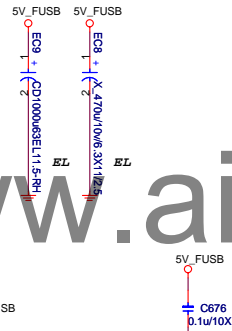
MS-7680

Size	Document Description	Rev
Custom	SATA / FAN Control	3.3
Date: Wednesday, June 08, 2011	Sheet 23. of 37	

5V_RUSB Switch

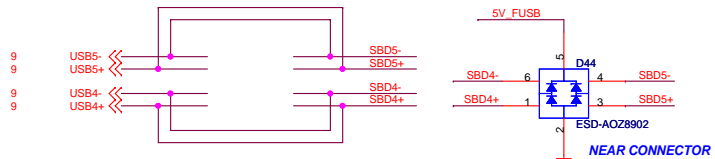


Front USB Connector

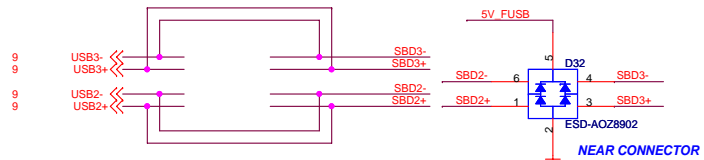


For H61 6,7,12,13 Port should be remove

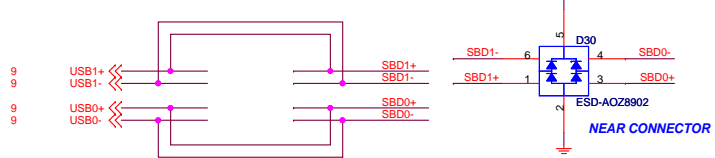
FRONT USB PORT 4,5



FRONT USB PORT 2,3

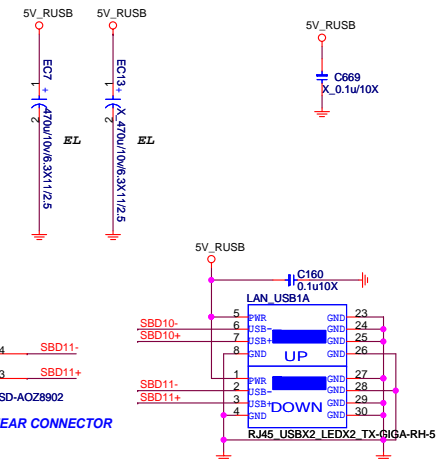


FRONT USB PORT 0,1

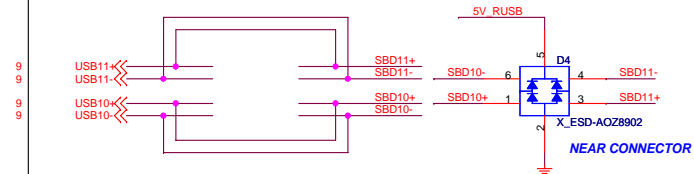


Rear USB Connector

NEAR USB REAR CONNECTOR



REAR USB PORT 10,11 (With LAN)

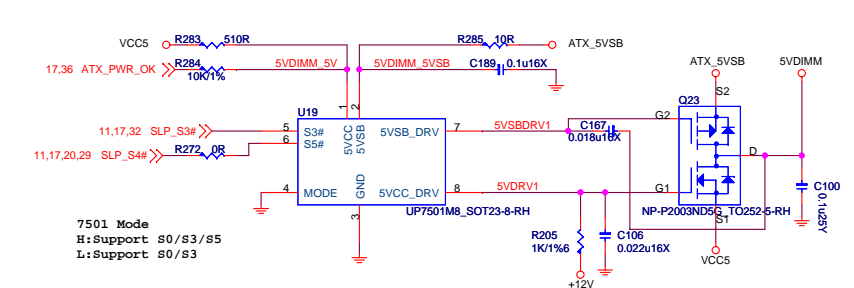


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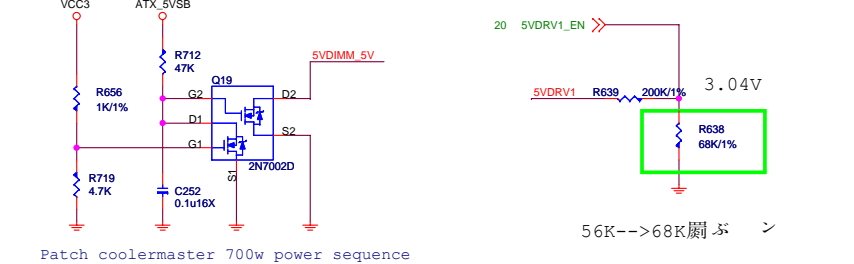
MS-7680

Size Custom	Document Description USB Connector	Rev 3.3
Date: Wednesday, June 08, 2011		Sheet 24 of 37

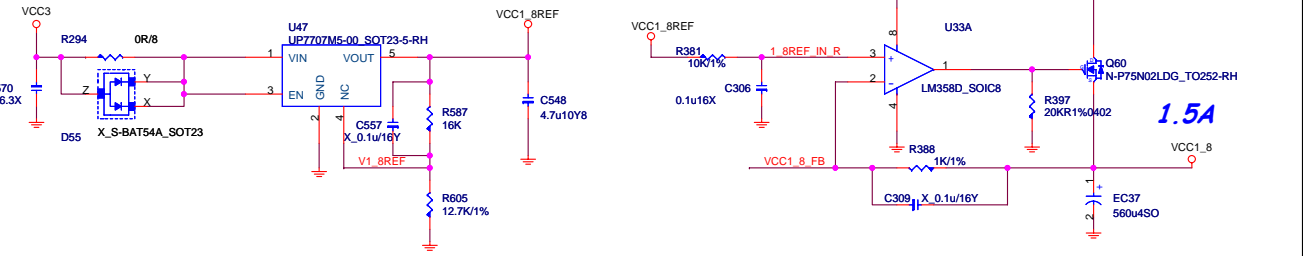
5VDIMM FOR DDR



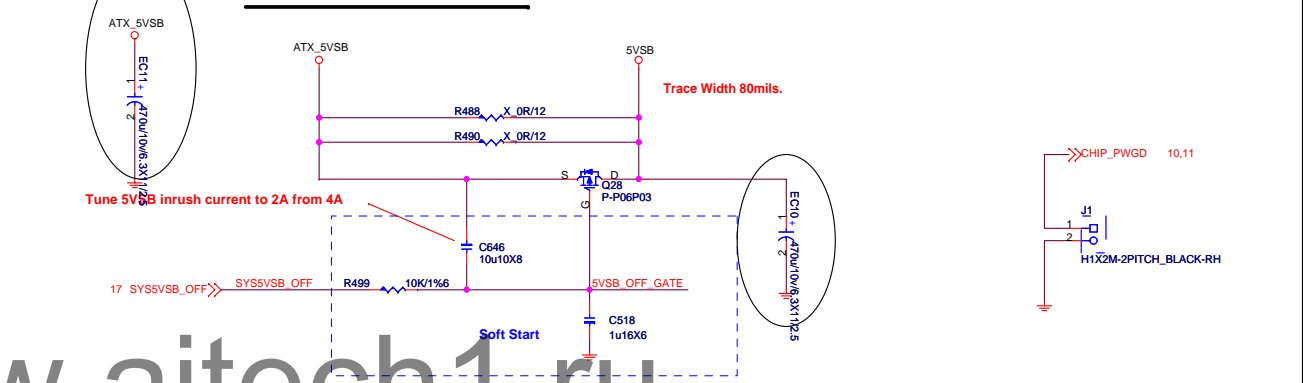
USB MODE



VCC1_8REF

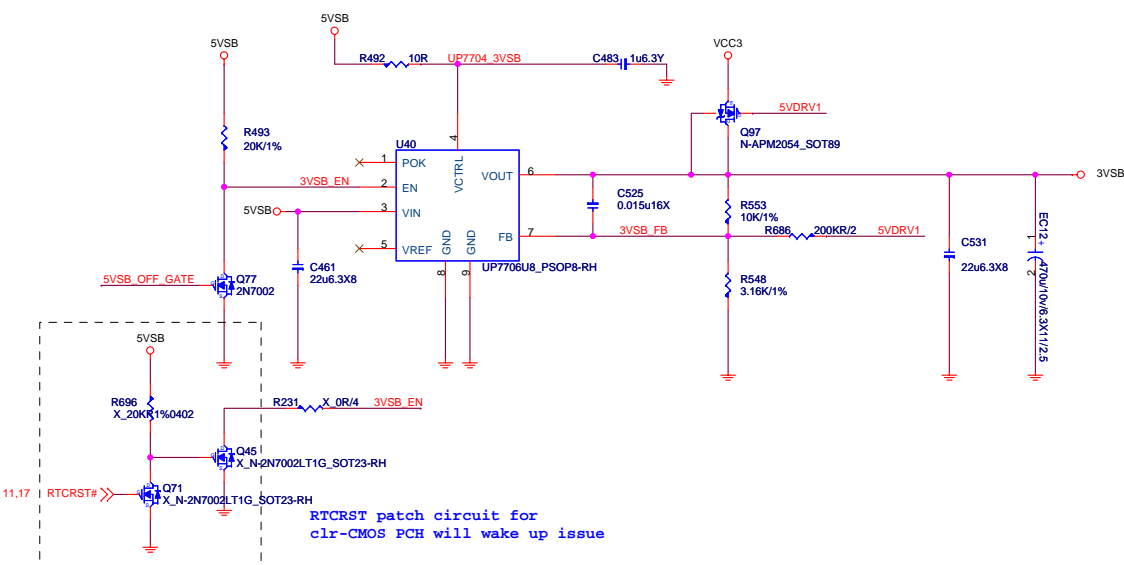


5VSB Power Switch



3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



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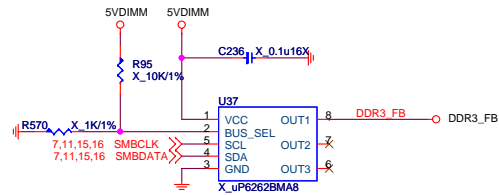
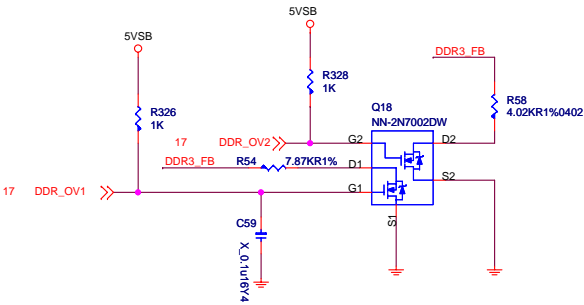
DDR3_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU

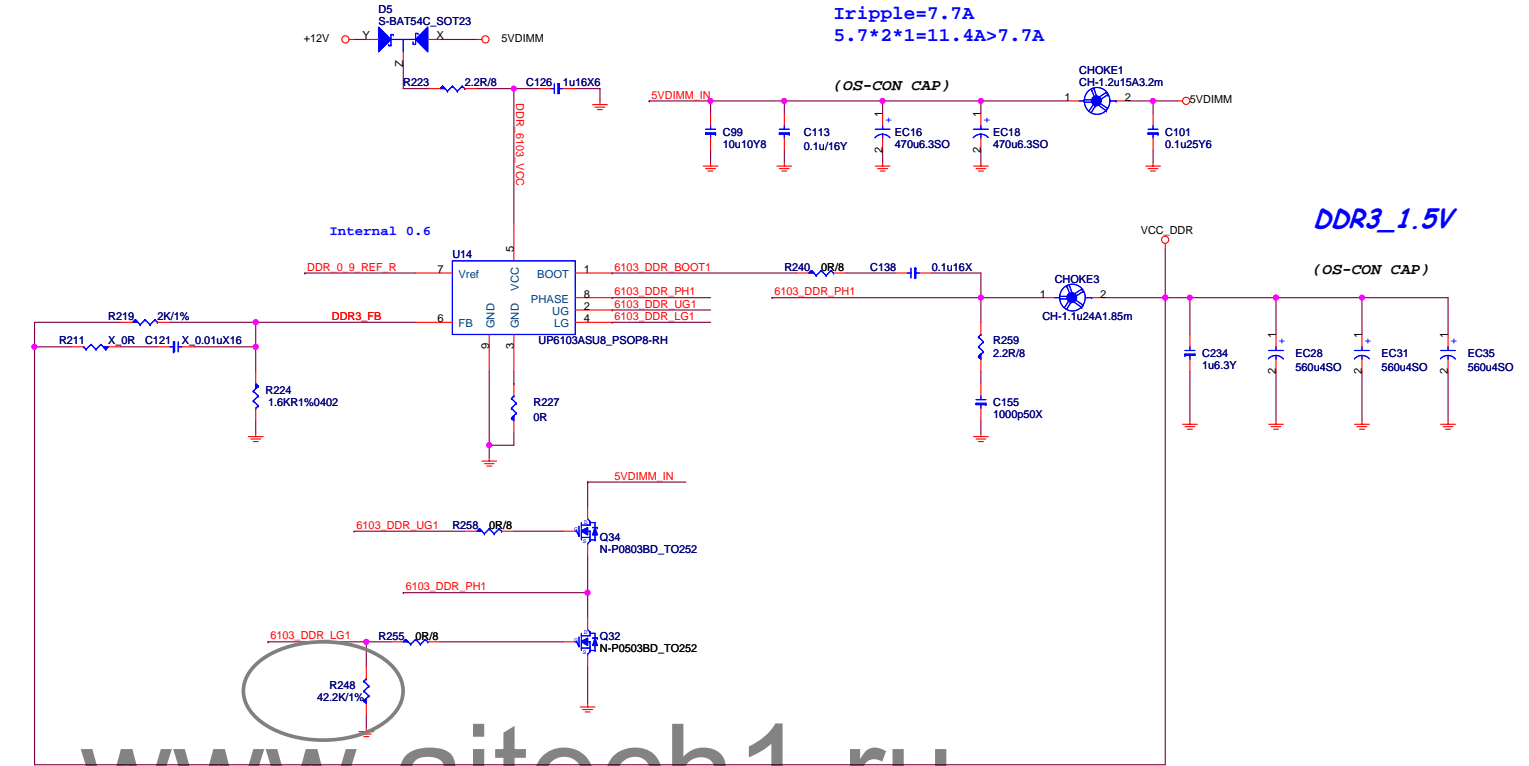
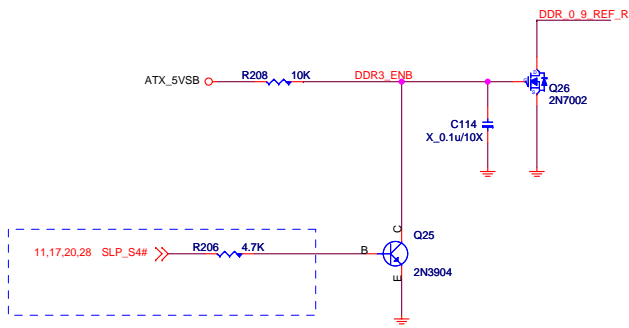
7.5A FOR 2DIMM

1A FOR DDR VTT

OV



P.S. Only for meet Intel power down sequence.



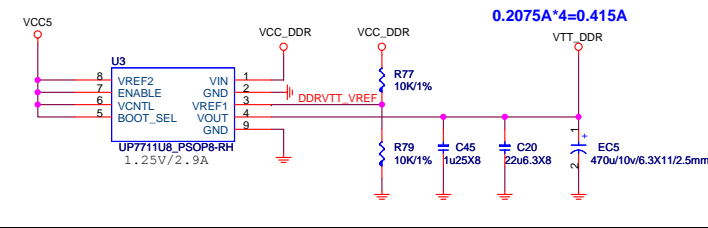
UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

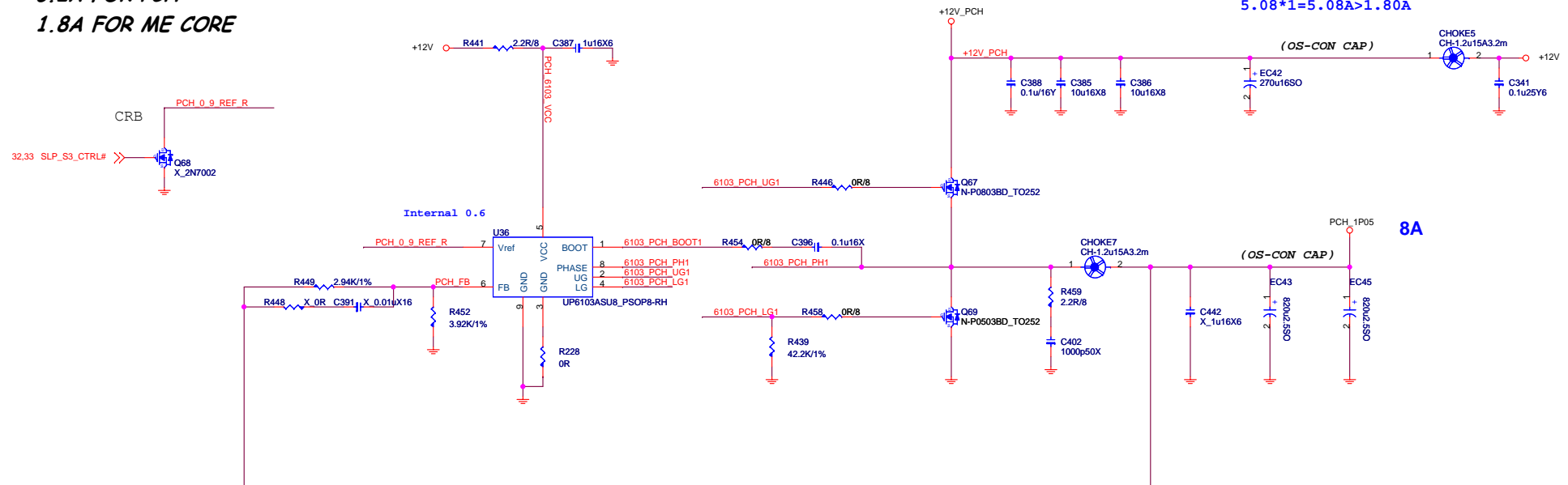


PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE



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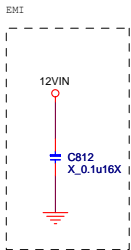
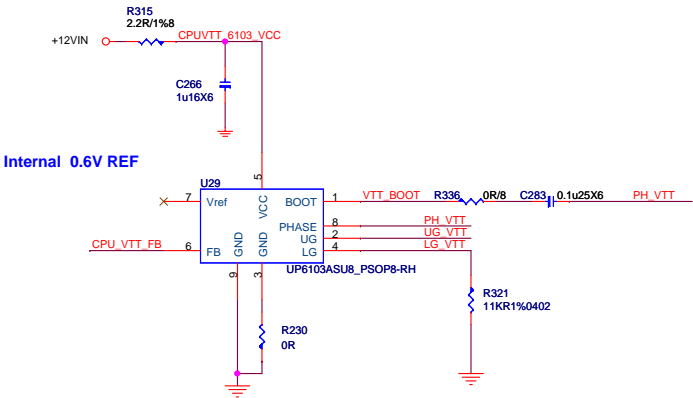
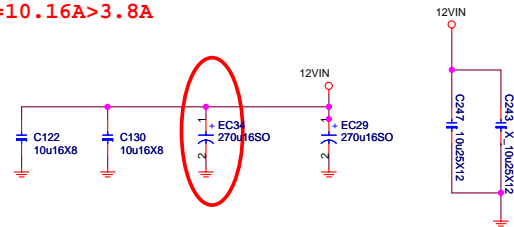
MS-7680

Size	Document Description	Rev
Custom	PCH Power - uP6103 1-Phase	3.3
Date:	Wednesday, June 08, 2011	Sheet 27 of 37

CPU_VTT:1.05/1.00

$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$

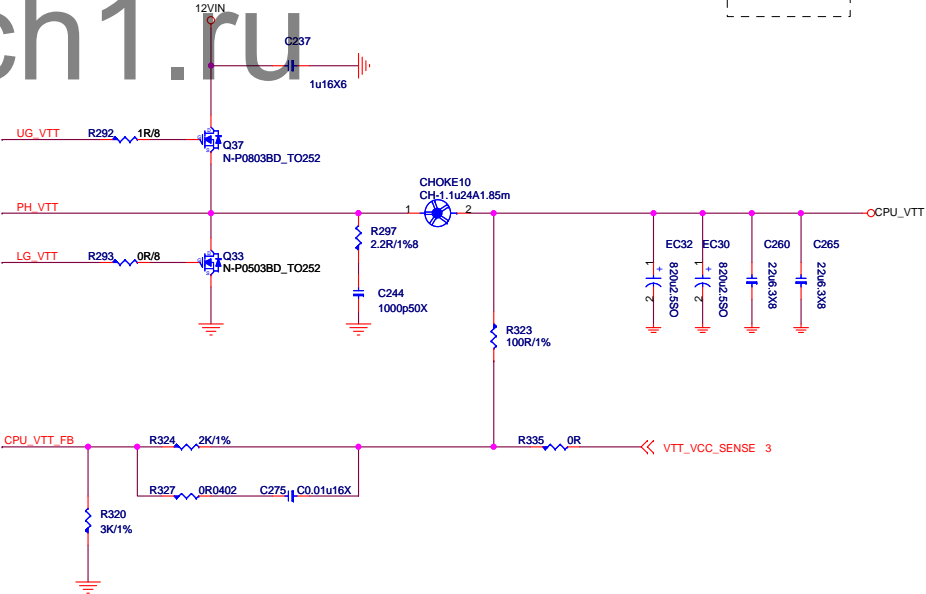
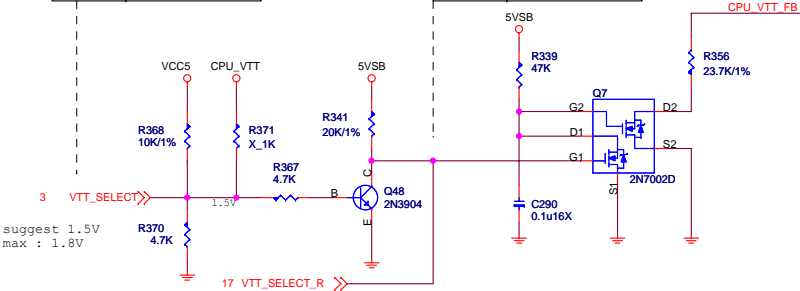
$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$
 $5.08 * 2 = 10.16A > 3.8A$



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VTT_SELECT	
Low	1.0V
High	1.05V

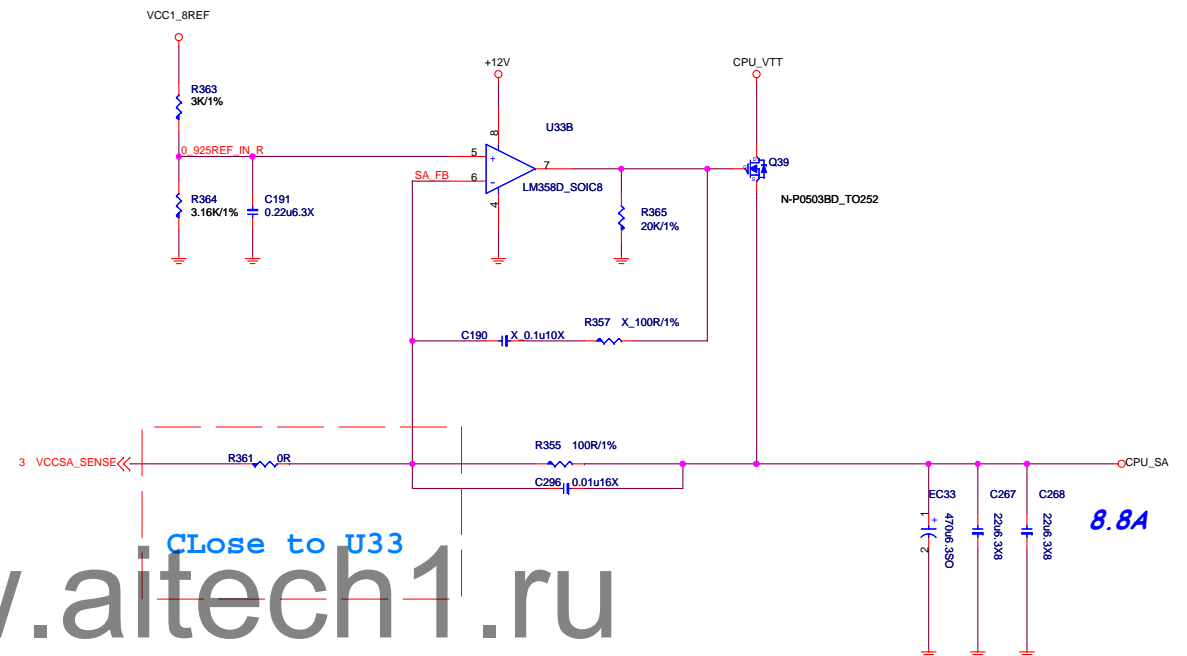
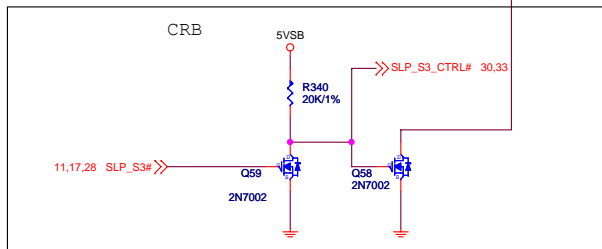
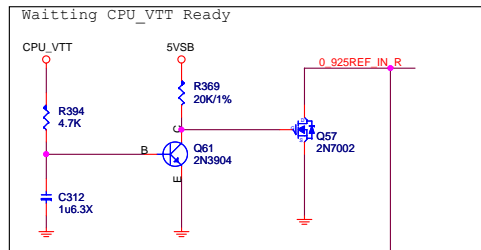
VTT_SELECT Table	
Low	1.05V
High	1.0V



MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size	Document Description	Rev
Custom	CPU_VTT - uP6103- 1-Phase	3.3
Date: Wednesday, June 08, 2011	Sheet 28 of 37	

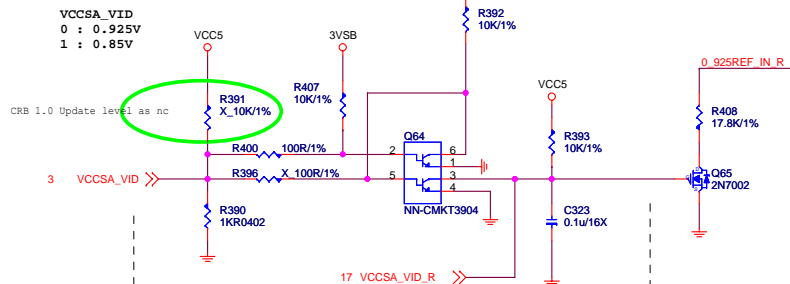
CPU_SA:0.925/0.85

SA Core =8.8A



Close to U33

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VCCSA_VID	
Low	0.925V
High	0.85V

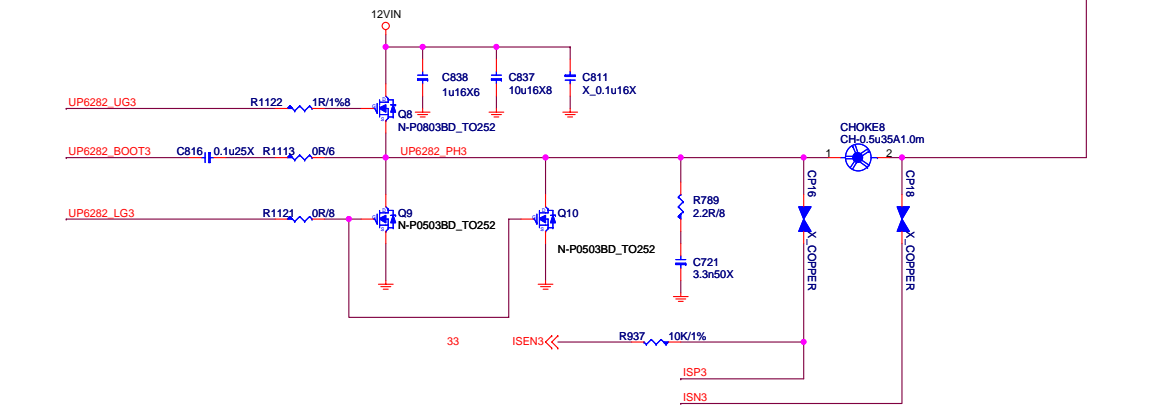
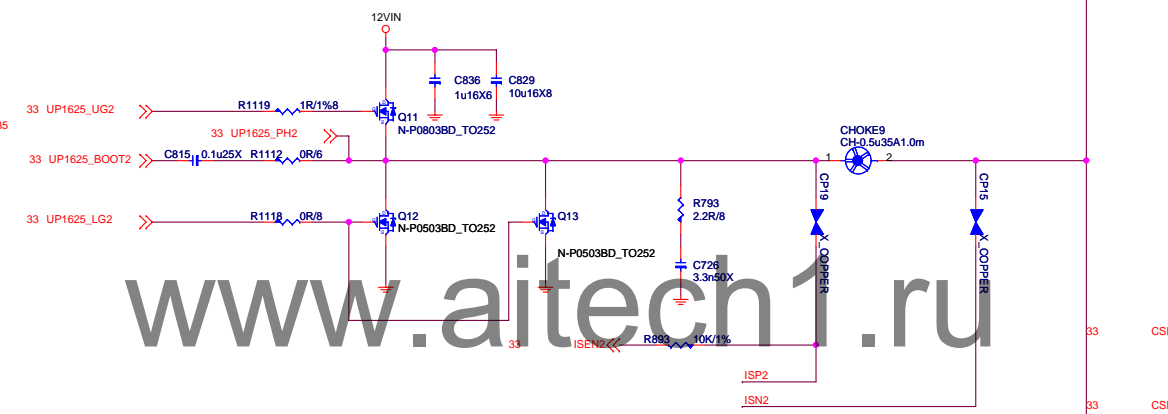
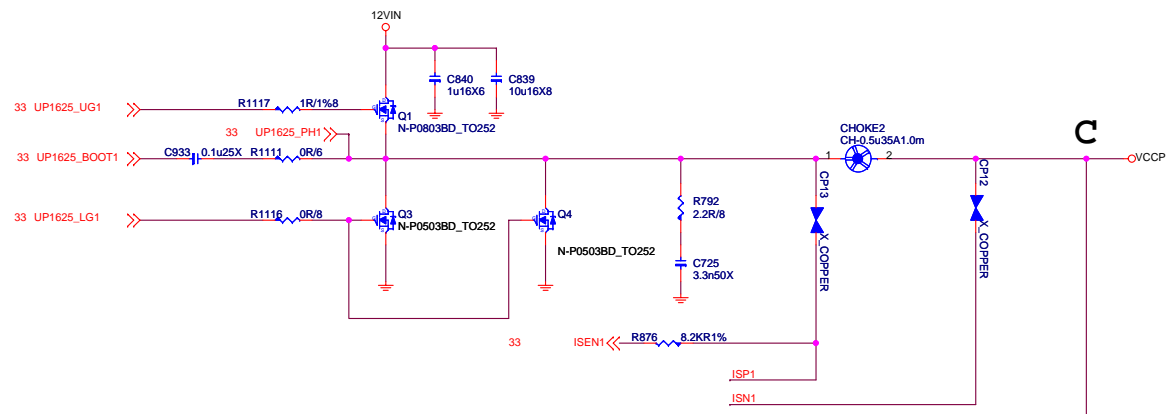
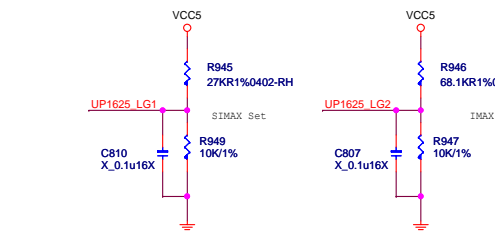
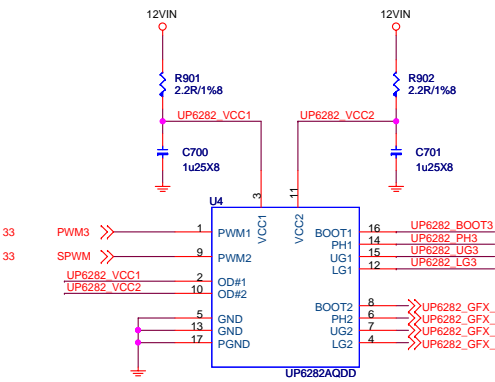
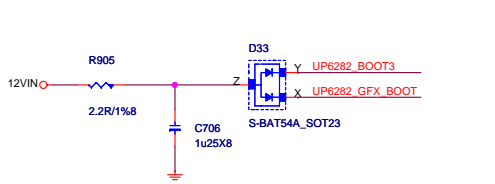
VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



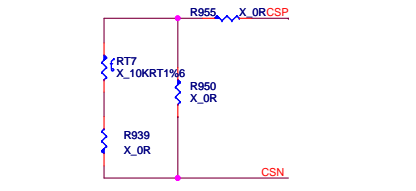
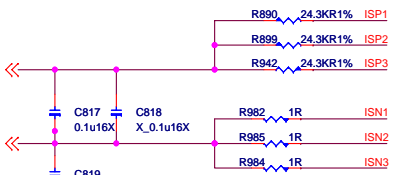
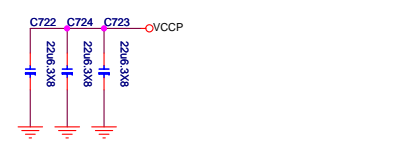
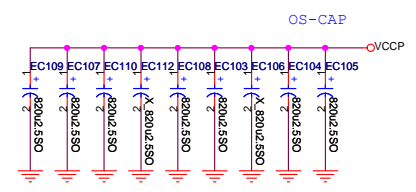
MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	CPU_SA - uP6103 1-Phase	3.3
Date: Wednesday, June 08, 2011		Sheet 29 of 37



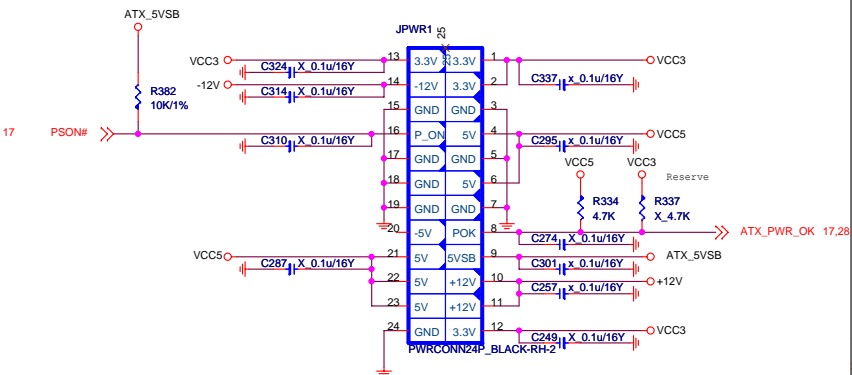
0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm



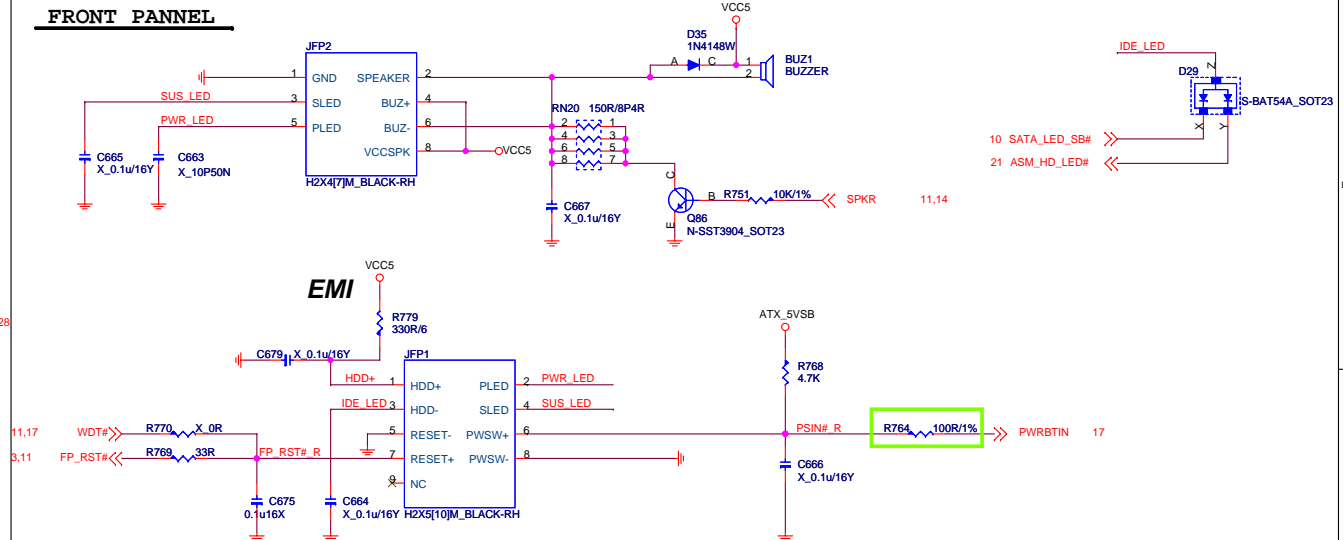
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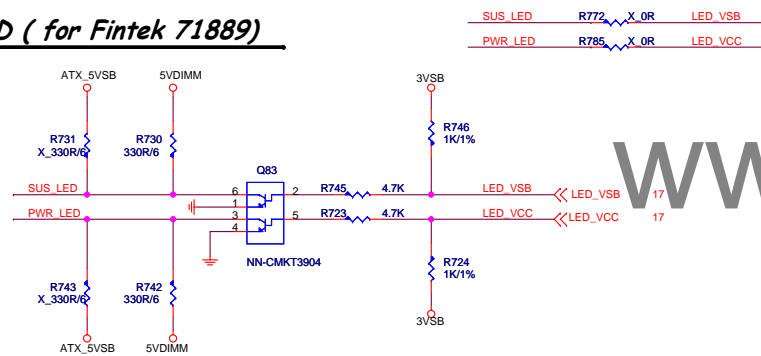
ATX POWER CONNECTOR



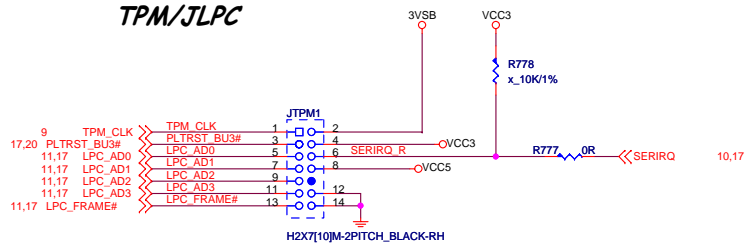
FRONT PANNEL



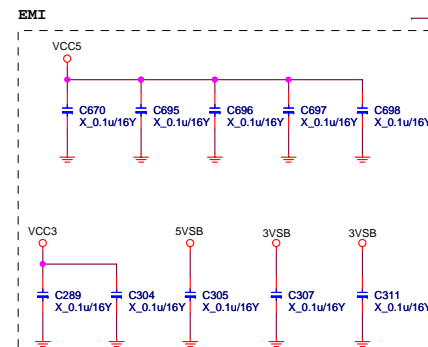
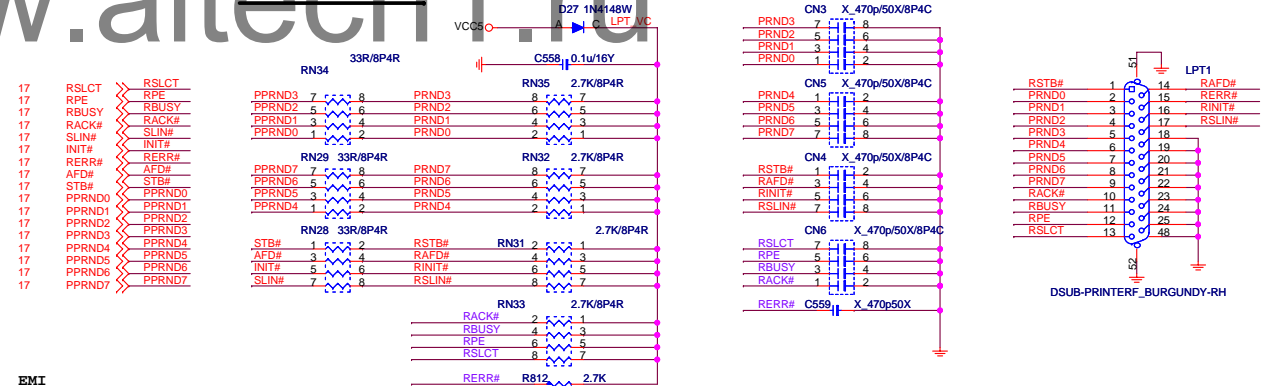
LED (for Fintek 71889)



TPM/JLPC



PARALLAL PORT



MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description
Custom	ATX PWR-Connector & Front Panel & EMI

Rev
3.3

Manual Parts

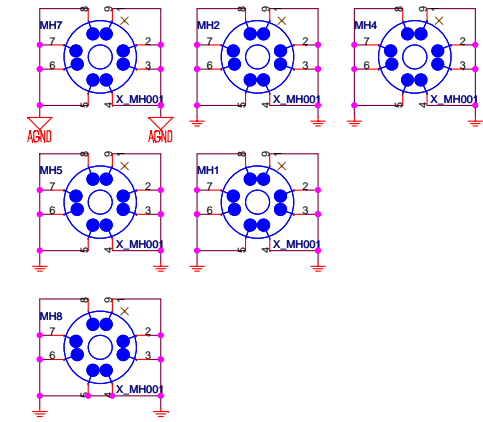
3IN1
OPT

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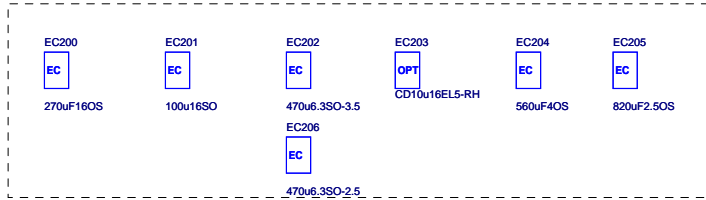
Simulation



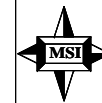
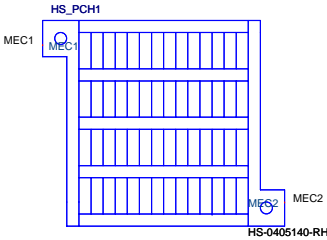
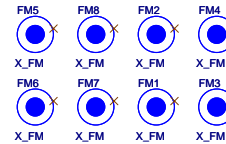
Mounting Holes



EL/OS OPT.



Optical Fiducial Marks-120



MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	XDP / Manual Parts	3.3
Date:	Wednesday, June 08, 2011	Sheet 34 of 37